1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD DATE | ENG APPD DATE |
|---|---|---|---|---|---|
| D | | 669438 | PRODUCTION RELEASED | 02/02/09 | |

# SCHEMATIC,MBP15","Contuba" MLB


| Page | (.csa) | Contents | Sync | Date |
|---|---|---|---|---|
| 1 | 1 | Table of Contents | N/A | N/A |
| 2 | 2 | System Block Diagram | T18_MLB | 12/12/2007 |
| 3 | 3 | Power Block Diagram | T18_MLB | 12/12/2007 |
| 4 | 4 | Power Block Diagram | N/A | N/A |
| 5 | 5 | BOM Configuration | N/A | N/A |
| 6 | 6 | JTAG Scan Chain | DDR | 07/22/2008 |
| 7 | 7 | Functional / ICT Test | N/A | N/A |
| 8 | 8 | Power Aliases | (MASTER) | (MASTER) |
| 9 | 9 | Signal Aliases | (MASTER) | (MASTER) |
| 10 | 10 | CPU FSB | M87_MLB | 10/17/2007 |
| 11 | 11 | CPU Power & Ground | M87_MLB | 10/17/2007 |
| 12 | 12 | CPU Decoupling & VID | M87_MLB | 10/17/2007 |
| 13 | 13 | eXtended Debug Port(MiniXDP) | M99_MLB | 01/08/2008 |
| 14 | 14 | MCP CPU Interface | T18_MLB | 06/18/2008 |
| 15 | 15 | MCP Memory Interface | T18_MLB | 06/18/2008 |
| 16 | 16 | MCP Memory Misc | T18_MLB | 06/18/2008 |
| 17 | 17 | MCP PCIe Interfaces | T18_MLB | 06/18/2008 |
| 18 | 18 | MCP Ethernet & Graphics | T18_MLB | 06/18/2008 |
| 19 | 19 | MCP PCI & LPC | T18_MLB | 06/18/2008 |
| 20 | 20 | MCP SATA & USB | T18_MLB | 06/18/2008 |
| 21 | 21 | MCP HDA & MISC | T18_MLB | 06/18/2008 |
| 22 | 22 | MCP Power & Ground | T18_MLB | 06/18/2008 |
| 23 | 24 | MCP79 A01 Silicon Support | T18_MLB | 03/31/2008 |
| 24 | 25 | MCP Standard Decoupling | T18_MLB | 06/18/2008 |
| 25 | 26 | MCP Graphics Support | AMASON_M98_MLB | 06/18/2008 |
| 26 | 28 | SB Misc | T18_MLB | 12/17/2007 |
| 27 | 29 | FSB/DDR3/FRAMEBUF Vref Margining | DDR | 07/22/2008 |
| 28 | 31 | DDR3 SO-DIMM Connector A | DDR | 07/22/2008 |
| 29 | 32 | DDR3 SO-DIMM Connector B | DDR | 07/22/2008 |
| 30 | 33 | DDR3 Support | T18_MLB | 06/18/2008 |
| 31 | 34 | Right Clutch Connector | YITE_M98_MLB | 07/02/2008 |
| 32 | 35 | ExpressCard Connector | YITE_M98_MLB | 07/02/2008 |
| 33 | 37 | Ethernet PHY (RTL8211CL) | SUMA_M98_MLB | 07/01/2008 |
| 34 | 38 | Ethernet & AirPort Support | SUMA_M98_MLB | 07/01/2008 |
| 35 | 39 | Ethernet Connector | SUMA_M98_MLB | 07/01/2008 |
| 36 | 41 | FireWire LLC/PHY (FW643) | SENSOR | 08/14/2008 |
| 37 | 42 | FireWire Port Power | K19_MLB | 11/02/2008 |
| 38 | 43 | FireWire Ports | SENSOR | 08/14/2008 |
| 39 | 45 | SATA Connectors | CHANG_M98_MLB | 07/01/2008 |
| 40 | 46 | External USB Connectors | AMASON_M98_MLB | 07/02/2008 |
| 41 | 48 | Front Flex Support | CHANG_M98_MLB | 07/01/2008 |
| 42 | 49 | SMC | T18_MLB | 06/18/2008 |
| 43 | 50 | SMC Support | AMASON_M98_MLB | 06/18/2008 |
| 44 | 51 | LPC+SPI Debug Connector | CHANG_M98_MLB | 07/01/2008 |
| 45 | 52 | M98 SMBus Connections | DDR | 07/22/2008 |
| 46 | 53 | Current & Voltage Sensing | SENSOR | 08/14/2008 |
| 47 | 54 | Current Sensing | SENSOR | 08/14/2008 |
| 48 | 55 | Thermal Sensors | SENSOR | 08/14/2008 |
| 49 | 56 | Fan Connectors | M87_MLB | 10/17/2007 |
| 50 | 57 | WELLSPRING 1 | AMASON_M98_MLB | 06/18/2008 |
| 51 | 58 | WELLSPRING 2 | PWRSQNC | 05/12/2008 |
| 52 | 59 | Sudden Motion Sensor (SMS) | SENSOR | 08/14/2008 |
| 53 | 61 | SPI ROM | CHANG_M98_MLB | 07/01/2008 |
| 54 | 62 | AUDIO:CODEC | AUDIO | 07/09/2008 |
| 55 | 63 | AUDIO: LINE IN | AUDIO | 07/09/2008 |
| 56 | 65 | AUDIO: HEADPHONE AMP | AUDIO | 07/09/2008 |
| 57 | 66 | AUDIO:SPEAKER AMP | AUDIO | 07/09/2008 |
| 58 | 67 | AUDIO: JACKS | AUDIO | 07/09/2008 |
| 59 | 68 | AUDIO: JACK TRANSLATORS | AUDIO | 07/09/2008 |
| 60 | 69 | DC-In & Battery Connectors | T18_MLB | 12/06/2007 |
| 61 | 70 | PBus Supply & Battery Charger | M99_MLB | 12/10/2007 |
| 62 | 71 | IMVP6 CPU VCore Regulator | M87_MLB | 10/17/2007 |
| 63 | 72 | 5V / 3.3V Power Supply | M99_MLB | 01/09/2008 |
| 64 | 73 | 1.5V DDR3 Supply | M99_MLB | 12/13/2007 |
| 65 | 75 | 5V_S0 / MCP Core Regulator | M99_MLB | 01/08/2008 |
| 66 | 76 | CPU VTT Power Supply | M99_MLB | 12/14/2007 |
| 67 | 77 | Misc Power Supplies | M99_MLB | 12/14/2007 |
| 68 | 78 | Power Control | PWRSQNC | 05/12/2008 |
| 69 | 79 | Power FETs | PWRSQNC | 05/12/2008 |
| 70 | 80 | NV G96 PCI-E | MUXGFX | 07/10/2008 |
| 71 | 81 | NV G96 Core/FB Power | MUXGFX | 07/10/2008 |
| 72 | 82 | NV G96 Frame Buffer I/F | MUXGFX | 07/10/2008 |
| 73 | 84 | GDDR3 Frame Buffer A (Top) | MUXGFX | 07/10/2008 |
| 74 | 85 | GDDR3 Frame Buffer B (Top) | MUXGFX | 07/10/2008 |
| 75 | 86 | NV G96 GPIO/MIO/Misc | MUXGFX | 07/10/2008 |
| 76 | 87 | G96 GPIOs & Straps | MUXGFX | 07/09/2008 |
| 77 | 88 | NV G96 Video Interfaces | MUXGFX | 07/10/2008 |
| 78 | 89 | GPU (G84M) Core Supply | M87_MLB | 10/17/2007 |
| 79 | 90 | LVDS Display Connector | MUXGFX | 02/25/2008 |
| 80 | 93 | Muxed Graphics Support | MUXGFX | 07/10/2008 |
| 81 | 94 | DisplayPort Connector | MUXGFX | 07/10/2008 |
| 82 | 95 | 1.1V / 1V8 FB Power Supply | MUXGFX | 07/10/2008 |
| 83 | 96 | Graphics MUX (GMUX) | MUXGFX | 07/10/2008 |
| 84 | 97 | LCD BACKLIGHT DRIVER | YITE_M98_MLB | 07/02/2008 |
| 85 | 98 | LCD Backlight Support | YITE_M98_MLB | 07/02/2008 |
| 86 | 99 | Misc Power Supplies | MUXGFX | 02/01/2008 |
| 87 | 100 | CPU/FSB Constraints | MUXGFX | 02/18/2008 |
| 88 | 101 | Memory Constraints | MUXGFX | 02/18/2008 |
| 89 | 102 | MCP Constraints 1 | MUXGFX | 02/18/2008 |
| 90 | 103 | MCP Constraints 2 | MUXGFX | 02/18/2008 |
| 91 | 104 | Ethernet Constraints | MUXGFX | 02/18/2008 |
| 92 | 105 | FireWire Constraints | MUXGFX | 02/18/2008 |
| 93 | 106 | SMC Constraints | MUXGFX | 02/18/2008 |
| 94 | 107 | GPU (G96) Constraints | MUXGFX | 02/18/2008 |
| 95 | 108 | Project Specific Constraints | MUXGFX | 02/21/2008 |
| 96 | 109 | PCB Rule Definitions | M99_MLB | 01/22/2008 |


02/02/2009

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 2 12:03:38 2009

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

| | | | |
|---|---|---|---|
| DRAFTER | | DESIGN CK | |
| ENG APPD | | MFG APPD | |
| QA APPD | | DESIGNER | |
| RELEASE | | SCALE | NONE |

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.


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TITLE
SCHEM,MBP 15MLB

DRAWING NUMBER 051-7902 REV. D

SHT 1 OF 109

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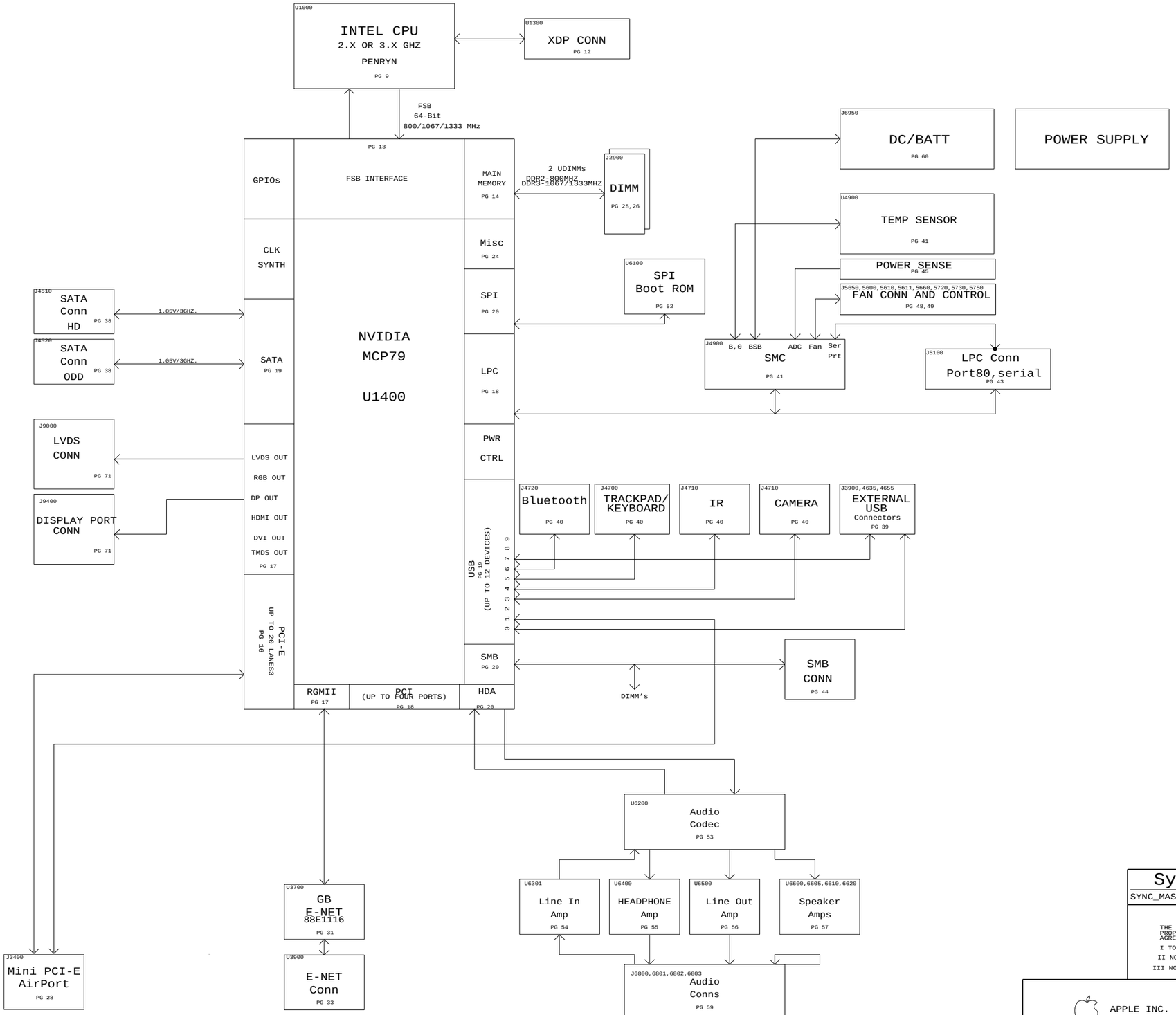


# System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007


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APPLE INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 2 | 109 |

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# M98A POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
6A FUSE
LIO_DCIN_ISENSE
U5705
CHGR_EN (S5)
ENABLES
VIN
VOUT
(PAGE 60)
PBUS SUPPLY/ BATTERY CHARGER
ISL6258A U7000

D6905
D6905
PPVIN_G3H_P3V42G3H
PBUSB_VSENSE
Q5315
8A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
ENABLE 3.425V G3HOT LT3470 U6990 (PAGE 59)
PP3V42_G3H_REG
SMC PWRGD RN5VD30A-E U5000 (PAGE 43)
SMC_RESET_L
SMC_GPU_VSENSE

U5498
GPU VCORE
VIN
VOUT
ISL6263B U8900
EN_PSV
PGOOD
(PAGE 78)
PM_GPUVCORE_EN
GPUVCORE_PGOOD
GPUVCORE_IOUT
PPVCORE_GPU_REG
(18A MAX CURRENT)

CPUVTTS0_EN
VIN
EN_PSV
VOUT
1.05V
TPS51117 U7600 (PAG 66)
PGOOD
PPCPUVTT_S0_REG
(6A MAX CURRENT)
CPUVTTS0_PGOOD
U2830
VR_PWRGD_CLKEN

MCP79
CK_PWRGD
VRMPWRGD
PWRBTN#
PLTRST*
RSMRST*
PWROK
CPUPWRGD(GPIO49)
U1400 (PAGE 14~22)
MCP_PS_PWRGD
U2850
CPU_PWRGD

U5715
SMC_BATT_ISENSE

U5400
SMC_CPU_VSENSE
CPU VCORE
VIN
VOUT
ISL9504B U7100
VR_ON
PGOOD
(PAGE 61)
IMVP_VR_ON_R
PPVCORE_CPU_S0
CPUVCORE_IOUT
VR_PWRGD_CLKEN_L
VR_PWRGOOD_DELAY

J6950
3S2P (9 TO 12.6V)
BATT_POS_F
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R

CPU PWRGOOD
U1000 (PAGE 10,11)
RESET*

PPBUS_G3H

Q7920
PP5V_S0_FET
P5VS0_SS
Q7900
PP5V_S3_FET
P5VS3_SS

MCP79
SLP_S5#(H47)
SLP_S3#(G47)
U1400 (PAGE 14~22)
P3V3S3_EN
P5VS3_EN
LIO_S3_EN

SMC
U4900
(PAGE 42)
P60(S5)
SMC_PM_G2_EN

P1V1GPU_EN
EN1 VIN
VOUT1
1.103V(L/H)
PP1V1_S0GPU_REG
P1V8FB_EN
EN2
VOUT2
1.8V(R/H)
PP1V8_GPU_REG
TPS51124 U9500 (PAGE 82)

U7859
VIN
5V (L/H)
VOUT1
PP5V_S5_REG
(8A MAX CURRENT)
3.3V (R/H)
VOUT2
PP3V3_S5_REG
(5.5A MAX CURRENT)
TPS51125 U7201 (PAGE 62)
EN0
PGOOD1,2
VREG3
P3V3S5_EN
P5V3V3_S5_PGOOD
PP5V_S3
PP3V3_S5

Q7910
P3V3S3_SS
PP3V3_S3_FET
PP3V3_S3
ISL8009 U7750 (PAGE 66)
V4
PP1V05_S5_MCP

U7400
VIN
EN/PSV
VOUT
SC417 (PAGE 64)
ENL
PGOOD
PP5V_RT_REG
P5V_RT_EN
P5V_RT_PGOOD

Q7930
PP3V3_S0GPU_FET
P3V3S0_SS
Q7970
PP3V3_S0_FET
P3V3GPU_SS
Q3810
P3V3_ENET_FET
P3V3ENET_EN_L

Q3805
WOW_EN
PM_WLAN_EN_L
Q3801
PM_ENET_EN
PM_ENET_EN_L
Q3800
WOL_EN
PM_ENET_EN_L
SMC_ADAPTER_EN
RC DELAY

U9701
GOSHAWK6P
VIN
ENA
VOUT
(PAGE 84)
BKLT_EN
PPVOUT_S0_LCDBKLT

VINLTC3407
RUN2
RUN1
VOUT1
VOUT2
U3850 (PAGE 33)
P1V2ENET_EN
ENETAVDD_EN
PP1V9_ENET_REG
PP1V2_ENET_REG

SMC
RSMRST_OUT(P15)
ALL_SYS_PWRGD
PWRGD(P12)→99ms DLY
RSMRST_PWRGD
SMC_ONOFF_L
PWR_BUTTON(P90)
P17(BTN_OUT)
RSMRST_IN(P13)
IMVP_VR_ON(P16)
PLT_RST*
RST*
PM_RSMRST_L
IMVP_VR_ON
PM_PWRBTN_L
SMC_RESET_L
P1V05S0_PGOOD
P5VRIGHT_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P1V8S0_PGOOD
P1V5S0_PGOOD
S0PGOOD_PWROK
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900 (PAGE 42)

PPVIN_S0_DDRREG_LDO
DDRREG_EN
DDRVTT_EN
PM_SLP_S3_L
VIN
VLDOIN
S5 1.8V
VOUT
S3 0.9V
VOUT
TPS51116 U7300 (PAGE 63)
PPDDR_S3_REG
(12A MAX CURRENT)
PPVTT_S0_DDR_LDO

RC DELAY
P5VRIGHT_EN
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P5VS0_EN (S0)
P3V3S0_EN (S0)
PBUSVSENS_EN (S0)
PM_SLP_S3_DELAY_L (S0)

MCP_CORE
EN2
VOUT2
1.1V
VOUT1
EN1
ISL6236 U7500 (PAGE 65)
VIN
MCPCORES0_EN
P1V05S0_EN
MCPCPCORE_S0_REG
(25A MAX CURRENT)
PP5V_RT_REG
(5A MAX CURRENT)

RST*
PP5V_S0
PP3V3_S0
PP1V5_S0_REG
V1
V2
V3
V4
LTC2900 U7870 (PAGE 68)

## Power Block Diagram

SYNC_MASTER=T18_MLB
SYNC_DATE=12/12/2007


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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 3 OF 109 | |

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# Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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|---|---|---|
| D | 051-7902 | D |
| SCALE | SHT | OF |
| NONE | 4 | 109 |

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# BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 630-9911 | PCBA,2.4GHZ,256SAM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6DZ,CPU_2_4GHZ,FB_256_SAMSUNG,AUDIO_HB |
| 630-9912 | PCBA,2.4GHZ,256HYN_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6EA,CPU_2_4GHZ,FB_256_HYNIX,AUDIO_HB |
| 630-9913 | PCBA,2.5GHZ,512SAM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6EB,CPU_2_5GHZ,FB_512_SAMSUNG,AUDIO_HB |
| 630-9914 | PCBA,2.5GHZ,512QIM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6EC,CPU_2_5GHZ,FB_512_QIMONDA,AUDIO_HB |
| 630-9915 | PCBA,2.8GHZ,512SAM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6ED,CPU_2_8GHZ,FB_512_SAMSUNG,AUDIO_HB |
| 630-9916 | PCBA,2.8GHZ,512QIM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6EE,CPU_2_8GHZ,FB_512_QIMONDA,AUDIO_HB |
| 630-9949 | PCBA,2.66GHZ,512SAM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6MT,CPU_2_66GHZ,FB_512_SAMSUNG,AUDIO_HB |
| 630-9950 | PCBA,2.66GHZ,512QIM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6MU,CPU_2_66GHZ,FB_512_QIMONDA,AUDIO_HB |
| 630-9951 | PCBA,2.93GHZ,512SAM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6N1,CPU_2_93GHZ,FB_512_SAMSUNG,AUDIO_HB |
| 630-9952 | PCBA,2.93GHZ,512QIM_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6N2,CPU_2_93GHZ,FB_512_QIMONDA,AUDIO_HB |
| 630-9956 | PCBA,2.5GHZ,512HYN_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6VG,CPU_2_5GHZ,FB_512_HYNIX,AUDIO_HB |
| 630-9957 | PCBA,2.66GHZ,512HYN_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6VH,CPU_2_66GHZ,FB_512_HYNIX,AUDIO_HB |
| 630-9958 | PCBA,2.8GHZ,512HYN_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6VJ,CPU_2_8GHZ,FB_512_HYNIX,AUDIO_HB |
| 630-9959 | PCBA,2.93GHZ,512HYN_VRAM,HB_AUDIO,M98A | M98_COMMON,EEE_6VK,CPU_2_93GHZ,FB_512_HYNIX,AUDIO_HB |

# Bar Code Labels / EEE #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6DZ] | CRITICAL | EEE_6DZ |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6EA] | CRITICAL | EEE_6EA |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6EB] | CRITICAL | EEE_6EB |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6EC] | CRITICAL | EEE_6EC |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6ED] | CRITICAL | EEE_6ED |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6EE] | CRITICAL | EEE_6EE |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6MT] | CRITICAL | EEE_6MT |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6MU] | CRITICAL | EEE_6MU |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6N1] | CRITICAL | EEE_6N1 |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6N2] | CRITICAL | EEE_6N2 |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6VG] | CRITICAL | EEE_6VG |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6VH] | CRITICAL | EEE_6VH |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6VJ] | CRITICAL | EEE_6VJ |
| 826-4393 | 1 | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:6VK] | CRITICAL | EEE_6VK |

# Alternates

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 138S0603 | 138S0602 | | ALL | Murata alt to Samsung |
| 353S1681 | 353S1294 | | ALL | LMV2011,OPAMP. GBW |
| 152S0276 | 152S0683 | | ALL | Maglayers alt to Dale/Vishay |
| 341S2367 | 341S2366 | | ALL | Macronix alt to SST |
| 152S0876 | 152S0867 | | ALL | Maglayer alt to Delta |
| 157S0058 | 157S0055 | | ALL | Delta alt to TDK Magnetics |
| 152S0915 | 152S0796 | | ALL | Maglayers alt to Cyntec IND |
| 128S0262 | 128S0220 | | ALL | Kemet alt to Sanyo |
| 127S0108 | 127S0062 | | ALL | Rohm alt to Kemet |
| 338S0714 | 338S0554 | | ALL | Low Leakage G96 GPU |

# Schematic / PCB #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-7902 | 1 | SCHEM,FIBBA,M98 | SCH | CRITICAL | |
| 820-2532 | 1 | PCBF,FIBBA,M98 | PCB | CRITICAL | |

# BOM Groups

| BOM GROUP | BOM OPTIONS |
|---|---|
| M98_COMMON | ALTERNATE,COMMON,M98_COMMON1,M98_COMMON2,M98_COMMON3,M98_DEBUG,M98_PROGPARTS |
| M98_COMMON1 | ONEWIRE_PU,ISL6258A,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_SMC |
| M98_COMMON2 | FW_LVG_NEW,BKLT_PLL_NOT,BMON_PROD,MIKEY,BOOT_MODE_USER,GPUVID_1P00V,MUXGFX |
| M98_COMMON3 | DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_HW,DP_CA_DET_EG_PLD,MCP_CS1_NO,NO_VREFMRGN,PROD_DIGSMS |
| M98_DEBUG | SMC_DEBUG_YES,XDP,LPCPLUS_NOT |
| M98_PROGPARTS | GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG |

| BOM GROUP | BOM OPTIONS |
|---|---|
| FB_256_SAMSUNG | VRAM4,VRAM_256_SAMSUNG |
| FB_256_HYNIX | VRAM4,VRAM_256_HYNIX |
| FB_512_SAMSUNG | VRAM4,VRAM_512_SAMSUNG |
| FB_512_HYNIX | VRAM4,VRAM_512_HYNIX |
| FB_512_QIMONDA | VRAM4,VRAM_512_QIMONDA |

# Module Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S3680 | 1 | IC,PDC,LGDZ,PRQ,2.40,25W,1066,R0,3M,BGA | U1000 | CRITICAL | CPU_2_4GHZ |
| 337S3681 | 1 | IC,PDC,SLGEK,PRQ,2.53,35W,1066,E0,6M,BGA | U1000 | CRITICAL | CPU_2_5GHZ |
| 337S3710 | 1 | IC,PDC,SLGEL,PRQ,2.66,35W,1066,E0,6M,BGA | U1000 | CRITICAL | CPU_2_66GHZ |
| 337S3682 | 1 | IC,PDC,SLGEM,PRQ,2.80,35W,1066,E0,6M,BGA | U1000 | CRITICAL | CPU_2_8GHZ |
| 337S3711 | 1 | IC,PDC,SLGEP,PRQ,2.93,35W,1066,E0,6M,BGA | U1000 | CRITICAL | CPU_2_93GHZ |
| 338S0635 | 1 | IC,GMCP,MCP79-B02,35x35MM,BGA1437 | U1400 | CRITICAL | MCP_B02 |
| 338S0710 | 1 | IC,MCP79XT-B3,35X35MM,BGA1437 | U1400 | CRITICAL | MCP_B03 |
| 338S0694 | 1 | IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P TQFP | U3700 | CRITICAL | |
| 338S0654 | 1 | IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12 | U4100 | CRITICAL | |
| 341S2384 | 1 | IR,ENCORE II, CY7C63803-LQXC | U4800 | CRITICAL | |
| 338S0563 | 1 | IC,SMC,HS8/2117,9MMX9MM,TLP | U4900 | CRITICAL | SMC_BLANK |
| 341S2448 | 1 | IC,SMC,DEVELOPMENT,M98 | U4900 | CRITICAL | SMC_PROG |
| 341S2383 | 1 | IC,PSOC +W/USB,56PIN,MLF,M98 | U5701 | CRITICAL | TPAD_PROG |
| 335S0384 | 1 | IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8 | U6100 | CRITICAL | BOOTROM_BLANK |
| 341S2447 | 1 | IC,EFI ROM,DEVELOPMENT,M98 | U6100 | CRITICAL | BOOTROM_PROG |
| 514-0612 | 1 | CONN,RCPT,S/PDIF,3.5MM,COMBO,XCVR,FL | J6700 | CRITICAL | AUDIO_NOHB |
| 514-0634 | 1 | CONN,RCPT,S/PDIF,3.5MM,COMBO,HB,FL | J6700 | CRITICAL | AUDIO_HB |
| 514-0613 | 1 | CONN,RCPT,S/PDIF,3.5MM,COMBO,RX,FL | J6750 | CRITICAL | AUDIO_NOHB |
| 514-0635 | 1 | CONN,RCPT,S/PDIF,3.5MM,COMBO,RX,HB,FL | J6750 | CRITICAL | AUDIO_HB |
| 353S2312 | 1 | IC,ISL6236C,DUAL PWM CNTl,QFN32 | U7500 | CRITICAL | |
| 338S0554 | 1 | IC,GPU,55nm,NV G96-GS,BGA969,LF | U8000 | CRITICAL | |
| 333S0482 | 4 | IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_256_SAMSUNG |
| 333S0483 | 4 | IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_256_HYNIX |
| 333S0481 | 4 | IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_512_SAMSUNG |
| 333S0506 | 4 | IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_512_HYNIX |
| 333S0472 | 4 | IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_512_QIMONDA |
| 341S2272 | 1 | IC,HDCP ROM,NVG96, 8 PIN SOIC,LF,HF | U8770 | CRITICAL | HDCP_YES |

# BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A


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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 5 OF 109 | |

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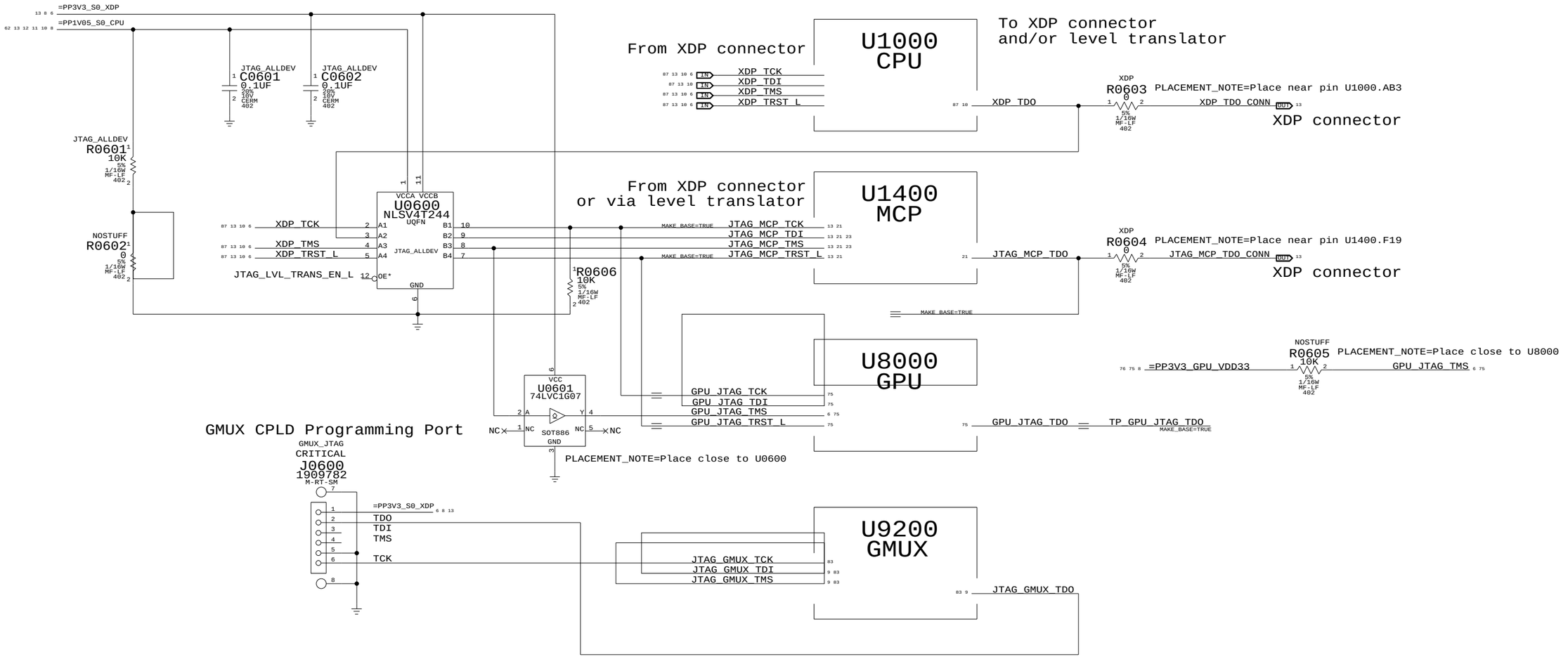
# 1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)




## JTAG Scan Chain

SYNC_MASTER=DDR SYNC_DATE=07/22/2008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|---|---|---|
| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 6 | 109 |

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# Functional Test Points

## Fan Connectors

FUNC_TEST

| | | | |
|---|---|---|---|
| TRUE | =PP5V_S0_FAN_LT | 8 49 | 3 TPs per Fan |
| TRUE | FAN_LT_PWM | 49 | |
| TRUE | FAN_LT_TACH | 49 | |
| TRUE | FAN_RT_PWM | 49 | |
| TRUE | FAN_RT_TACH | 49 | |
| TRUE | GND | | 5 TPs per Fan |

## LVDS Connectors

FUNC_TEST

| | | | |
|---|---|---|---|
| TRUE | =PP3V3_S0_DDC_LCD | 8 76 79 | |
| TRUE | PP3V3_SW_LCD | 79 | |
| TRUE | BKL_SYNC | 79 84 | |
| TRUE | LVDS_DDC_CLK | 79 80 | |
| TRUE | LVDS_DDC_DATA | 79 80 | |
| TRUE | LVDS_CONN_A_DATA_N<0> | 79 80 94 | |
| TRUE | LVDS_CONN_A_DATA_P<0> | 79 80 94 | |
| TRUE | LVDS_CONN_A_DATA_N<1> | 79 80 94 | |
| TRUE | LVDS_CONN_A_DATA_P<1> | 79 80 94 | |
| TRUE | LVDS_CONN_A_DATA_N<2> | 79 80 94 | |
| TRUE | LVDS_CONN_A_DATA_P<2> | 79 80 94 | |
| TRUE | LVDS_CONN_A_CLK_F_N | 79 94 | |
| TRUE | LVDS_CONN_A_CLK_F_P | 79 94 | |
| TRUE | LVDS_CONN_B_DATA_N<0> | 79 80 94 | |
| TRUE | LVDS_CONN_B_DATA_P<0> | 79 80 94 | |
| TRUE | LVDS_CONN_B_DATA_N<1> | 79 80 94 | |
| TRUE | LVDS_CONN_B_DATA_P<1> | 79 80 94 | |
| TRUE | LVDS_CONN_B_DATA_N<2> | 79 80 94 | |
| TRUE | LVDS_CONN_B_DATA_P<2> | 79 80 94 | |
| TRUE | LVDS_CONN_B_CLK_F_N | 79 94 | |
| TRUE | LVDS_CONN_B_CLK_F_P | 79 94 | |
| TRUE | LED_RETURN_1 | 79 84 | |
| TRUE | LED_RETURN_2 | 79 84 | |
| TRUE | LED_RETURN_3 | 79 84 | |
| TRUE | LED_RETURN_4 | 79 84 | |
| TRUE | LED_RETURN_5 | 79 84 | |
| TRUE | LED_RETURN_6 | 79 84 | |

## EXCARD Connector

FUNC_TEST

| | | |
|---|---|---|
| TRUE | USB2_EXCARD_CONN_N | 32 95 |
| TRUE | USB2_EXCARD_CONN_P | 32 95 |
| TRUE | PCIE_CLK100M_EXCARD_CONN_N | 32 95 |
| TRUE | PCIE_CLK100M_EXCARD_CONN_P | 32 95 |
| TRUE | PCIE_EXCARD_R2D_N | 32 89 95 |
| TRUE | PCIE_EXCARD_R2D_P | 32 89 95 |
| TRUE | PCIE_EXCARD_D2R_P | 17 32 89 |
| TRUE | PCIE_EXCARD_D2R_N | 17 32 89 |
| TRUE | PP3V3_S3_EXCARD_SWITCH | 32 |
| TRUE | PP3V3_S0_EXCARD_SWITCH | 32 |
| TRUE | PP1V5_S0_EXCARD_SWITCH | 32 |
| TRUE | PLT_RESET_SWITCH_L | 32 |
| TRUE | EXCARD_CPPE_L | 32 |
| TRUE | EXCARD_CPUSB_L | 32 |
| TRUE | EXCARD_CLKREQ_CONN_L | 32 |
| TRUE | SMBUS_MCP_0_CLK | 13 21 45 90 |
| TRUE | SMBUS_MCP_0_DATA | 13 21 45 90 |

## Speaker Connectors

FUNC_TEST

| | | |
|---|---|---|
| TRUE | BI_MIC_LO | 58 59 |
| TRUE | BI_MIC_SHIELD | 58 59 |
| TRUE | BI_MIC_HI | 58 59 |
| TRUE | SPKRCONN_L_P_OUT | 57 58 95 |
| TRUE | SPKRCONN_L_N_OUT | 57 58 95 |
| TRUE | SPKRCONN_R_P_OUT | 57 58 95 |
| TRUE | SPKRCONN_R_N_OUT | 57 58 95 |
| TRUE | SPKRCONN_S_P_OUT | 57 58 95 |
| TRUE | SPKRCONN_S_N_OUT | 57 58 95 |
| TRUE | GND | 6 TPs |

## SATA ODD Connectors

FUNC_TEST

| | | | |
|---|---|---|---|
| TRUE | PP5V_SW_ODD | 39 | 4 TPs |
| TRUE | SMC_ODD_DETECT | 39 42 | |
| TRUE | SATA_ODD_R2D_P | 39 89 | |
| TRUE | SATA_ODD_R2D_N | 39 89 | |
| TRUE | SATA_ODD_D2R_C_N | 39 89 | |
| TRUE | SATA_ODD_D2R_C_P | 39 89 | |
| TRUE | GND | | 5 TPs |

## POWER RAILS

| | | |
|---|---|---|
| TRUE | PM_SLP_S3_L | 21 34 37 42 44 68 81 83 |
| TRUE | PPBUS_G3H | 8 46 |
| TRUE | PPBUS_CPU_IMVP_ISNS | 8 |
| TRUE | PP3V42_G3H | 7 8 43 |
| TRUE | PP5V_S3 | 8 |
| TRUE | PP5V_S0 | 8 |
| TRUE | PPVCORE_S0_CPU | 8 |
| TRUE | PPVCORE_S0_MCP_REG | 8 |
| TRUE | PPVCORE_S0_MCP | |
| TRUE | PP3V3_S5 | 8 95 |
| TRUE | PP3V3_S3 | 8 |
| TRUE | PP3V3_S0 | 8 95 |
| TRUE | PP2V5_S0 | 8 |
| TRUE | PP1V2_S0 | 8 |
| TRUE | PP1V8_S0 | 8 |
| TRUE | PP1V8R1V5_S3 | 8 |
| TRUE | PP1V8R1V5_S0_FET | 8 |
| TRUE | PPMCPDDR_ISNS | 8 |
| TRUE | PP1V05_S0_REG | 8 |
| TRUE | PP1V2R1V05_S5 | 8 |
| TRUE | PPCPUVTT_S0 | 8 |
| TRUE | PPCPUFSB_ISNS_R | 8 |
| TRUE | PP0V9R0V75_S0_DDRVTT | 8 |
| TRUE | PP1V2R1V05_ENET | 8 |
| TRUE | PP3V3_ENET_PHY | 8 |
| TRUE | PPVP_FW | 8 |
| TRUE | PP1V0_FW | 8 |
| TRUE | PP3V3_S0GPU | 8 |
| TRUE | PP1V1_S0GPU_REG | 8 |
| TRUE | PP1V8_S0GPU_ISNS | 8 |
| TRUE | PPVCORE_GPU | 8 |
| TRUE | PP1V8_S0GPU_ISNS_R | 8 |
| TRUE | PP3V3_S5_AVREF_SMC | 42 43 |
| TRUE | PPVOUT_S0_LCDBKLT | 79 84 |
| TRUE | PPDCIN_G3H | 8 |
| TRUE | PPVTTDDR_S3 | 8 |
| TRUE | PP1V8_GPUIFPX | 8 |

# ICT Test Points

## CPU FSB NO_TESTs

NO_TEST

| | | |
|---|---|---|
| TRUE | FSB_A_L<31..3> | 10 14 87 |
| TRUE | FSB_ADS_L | 10 14 87 |
| TRUE | FSB_ADSTB_L<1..0> | 10 14 87 |
| TRUE | FSB_D_L<63..0> | 10 14 87 |
| TRUE | FSB_DINV_L<3..0> | 10 14 87 |
| TRUE | FSB_DSTB_L_N<3..0> | 10 14 87 |
| TRUE | FSB_DSTB_L_P<3..0> | 10 14 87 |
| TRUE | FSB_HIT_L | 10 14 87 |
| TRUE | FSB_HITM_L | 10 14 87 |
| TRUE | FSB_LOCK_L | 10 14 87 |
| TRUE | FSB_REQ_L<4..0> | 10 14 87 |

## IPD_FLEX_CONN

| | | |
|---|---|---|
| TRUE | PP3V3_S3_LDO | 51 |
| TRUE | PP18V5_S3 | 51 |
| TRUE | TPAD_GND_F | 7 51 |
| TRUE | Z2_CS_L | 50 51 |
| TRUE | Z2_DEBUG3 | 50 51 |
| TRUE | Z2_MOSI | 50 51 |
| TRUE | Z2_MISO | 50 51 |
| TRUE | Z2_SCLK | 50 51 |
| TRUE | Z2_BOOST_EN | 51 |
| TRUE | Z2_HOST_INTN | 50 51 |
| TRUE | Z2_BOOT_CFG1 | 50 51 |
| TRUE | Z2_CLKIN | 50 51 |
| TRUE | Z2_KEY_ACT_L | 50 51 |
| TRUE | Z2_RESET | 50 51 |
| TRUE | PSOC_MISO | 50 51 |
| TRUE | PSOC_MOSI | 50 51 |
| TRUE | PSOC_SCLK | 50 51 |
| TRUE | SMBUS_SMC_A_S3_SDA | 45 93 |
| TRUE | SMBUS_SMC_A_S3_SCL | 45 93 |
| TRUE | PSOC_F_CS_L | 50 51 |
| TRUE | PICKB_L | 50 51 |

## KEYBOARD CONN

| | | |
|---|---|---|
| TRUE | PP3V42_G3H | 7 8 43 |
| TRUE | WS_KBD1 | 50 |
| TRUE | WS_KBD2 | 50 |
| TRUE | WS_KBD3 | 50 |
| TRUE | WS_KBD4 | 50 |
| TRUE | WS_KBD5 | 50 |
| TRUE | WS_KBD6 | 50 |
| TRUE | WS_KBD7 | 50 |
| TRUE | WS_KBD8 | 50 |
| TRUE | WS_KBD9 | 50 |
| TRUE | WS_KBD10 | 50 |
| TRUE | WS_KBD11 | 50 |
| TRUE | WS_KBD12 | 50 |
| TRUE | WS_KBD13 | 50 |
| TRUE | WS_KBD14 | 50 |
| TRUE | WS_KBD15_CAP | 50 |
| TRUE | WS_KBD16_NUM | 50 |
| TRUE | WS_KBD17 | 50 |
| TRUE | WS_KBD18 | 50 |
| TRUE | WS_KBD19 | 50 |
| TRUE | WS_KBD20 | 50 |
| TRUE | WS_KBD21 | 50 |
| TRUE | WS_KBD22 | 50 |
| TRUE | WS_KBD23 | 50 |
| TRUE | WS_KBD_ONOFF_L | 50 |
| TRUE | WS_LEFT_SHIFT_KBD | 50 |
| TRUE | WS_LEFT_OPTION_KBD | 50 |
| TRUE | WS_CONTROL_KBD | 50 |
| TRUE | KBDLED_ANODE | 51 |
| TRUE | TPAD_GND_F | 7 51 |

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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## "G3Hot" (Always-Present) Rails

=PPBUS_G3H (61) → PPBUS_G3H (7, 46)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

- =PPVIN_S5_P5VP3V3 (63)
- =PPVIN_S0_CPUVTTS0 (66)
- =PPBUS_S0_LCDBKLT (85)
- =PPBUS_S5_FWPWRSW (37)
- =PPVIN_GPU_GPUVCORE (78)
- =PPVIN_S5_CPU_IMVP_ISNS_R (46)
- =PPVIN_S0_P5VRTS0_MCPCORE (65)
- =PPVIN_S3_DDRREG (64)
- =PPVIN_S0GPU_P1V8P1V1 (82)
- =PPVBAT_G3H_P3V42G3H (60)
- =PPVIN_S0_P1V05S5 (67)

=PPVIN_S5_CPU_IMVP_ISNS (46) → PPBUS_CPU_IMVP_ISNS (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

- =PPVIN_S5_CPU_IMVP (62)

=PP18V5_DCIN_CONN (60) → PPDCIN_G3H (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

- =PPDCIN_S5_CHGR (61)

=PP3V42_G3H_REG (60) → PP3V42_G3H (7, 43)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

- =PP3V42_G3H_SMCUSBMUX (40)
- =PP3V42_G3H_SMBUS_SMC_BSA (45)
- =PP3V3_S5_SMC (42, 43, 52)
- =PP3V3_S5_LPCPLUS (44)
- =PPVIN_S5_SMCVREF (43)
- =PP3V42_G3H_PWRCTL (63, 68)
- =PP3V42_G3H_CHGR (61)
- =PP3V3_S5_RTC_D (26)
- =PP3V42_G3H_BATT (60)
- =PP3V42_G3H_TPAD (50)
- =PP3V42_G3H_BMON_ISNS (46)
- =PP3V42_G3H_CPUCOREISNS (46)

## 5V Rails

=PP5V_S3_REG (63) → PP5V_S3 (7)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S3_SYSLED (43)
- =PP5V_S3_BTCAMERA (31)
- =PP5V_S3_WLAN (31)
- =PP5V_S3_IR (41)
- =PP5V_S3_DDRREG (64)
- =PP5V_S3_GPUVCORE (78)
- =PP5V_S3_RTUSB (40)
- =PP5V_S3_TPAD (51)
- =PP5V_S3_P1V05S0FET (69)
- =PP5V_S3_MCPDDRFET (69)
- =PP5V_S3_VTTCLAMP (69)
- =PP5V_S3_AUDIO_PWR (9)

=PP5V_RT_REG (65) → PP5V_S0 (7)
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S0_FAN_LT (7, 49)
- =PP5V_S0_FAN_RT (49)
- =PP5V_S0_CPU_IMVP (62)
- =PP5V_S0_CPUVTTS0 (66)
- =PP5V_S0_KBDLED (51)
- =PP5V_S0GPU_P1V1P1V8_GPU (82)
- =PP5V_S0_LPCPLUS (44)
- =PP5V_S0_ODD (39)
- =PP5V_S0_HDD (39)

## Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG (62) → PPVCORE_S0_CPU (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

- =PPVCORE_S0_CPU (11, 12, 46)

=PPMCPCORE_S0_REG (65) → PPVCORE_S0_MCP_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PPVCORE_S0_MCP (22, 24, 46)

## 3.3V-2.5V Rails

=PP3V3_S5_REG (63) → PP3V3_S5 (7, 95)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S5_MCP_A01 (23, 44)
- =PP3V3_S5_ROM (44, 53)
- =PP3V3_S5_MEMRESET (30)
- =PP3V3_S3_P3V3S3FET (69)
- =PP3V3_S5_LCD (79)
- =PP3V3_S0_P3V3S0FET (69)
- =PP3V3_GPU_P3V3GPUFET (69)
- =PP3V3_S5_PWRCTL (68)
- =PP3V3_S5_P1V05FET (69)
- =PP3V3_S5_MCP (22, 24)
- =PP3V3_S5_MCP_GPIO (18, 20)
- =PP3V3_FW_LATEVG_ACTIVE (37)
- =PP3V3_S5_MCPPWRGD (26)
- =PP3V3_FW_LATEVG (38)
- =PP3V3_S5_P1V05ENETFET (34)
- =PP3V3_S5_P3V3ENETFET (34)
- =PP3V3_S5_DP_PORT_PWR (81)

=PP3V3_S3_FET (69) → PP3V3_S3 (7)
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_FW_REG (8)
- =PP3V3_S3_SMBUS_SMC_A_S3 (45)
- =PP3V3_S3_SMS (52)
- =PP3V3_S3_REMTHMSNS (48)
- =PP3V3_S3_TPAD (50)
- =PP3V3_S3_WLAN (31)
- =PP3V3_S3_MCP_GPIO (21)
- =PP3V3_S3_VREFMRGN (27)
- =PP3V3_S3_SMBUS_SMC_MGMT (45)
- =PP3V3_S3_EXCARD (32)
- =PP3V3_S3_P1V8S0 (67)

=PP3V3_S0_FET (69) → PP3V3_S0 (7, 95)
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S0_LPCPLUS (44)
- =PP3V3_S0_SMC (43)
- =PP3V3_S0_SMBUS_SMC_B_S0 (45)
- =PP3V3_S0_MCPDDRISNS (47)
- =PP3V3_S0_GPU1V8ISNS (47)
- =PP3V3_S0_CPUTHMSNS (48)
- =PP3V3_S0_GPUTHMSNS (48)
- =PP3V3_S0_FAN_LT (49)
- =PP3V3_S0_FAN_RT (49)
- =PP3V3_S0_IMVP (62)
- =PP3V3_S0_PWRCTL (68)
- =PP3V3_S0_DDC_LCD (7, 76, 79)
- =PP3V3_S0_XDP (6, 13)
- =PP3V3_S0_MCPCOREISNS (47)
- =PPSPD_S0_MEM_A (28)
- =PPSPD_S0_MEM_B (29)
- =PP3V3_FW_FWPHY (8, 36, 38)
- =PP3V3_FW_P1V0FW (67)
- =PP3V3_S0_SMBUS_MCP_0 (45)
- =PP3V3_S0_GMUX (83)
- =PP3V3_S0_DPMUX (80)
- =PP3V3_S0_DPCONN (81)
- =PP3V3_S0_P1V2P2V5 (86)
- =PP3V3_S0_MCP_GPIO (18, 19, 21)
- =PP3V3_S0_HDCPROM (25)
- =PP3V3R1V5_S0_MCP_HDA (21, 24)
- =PP3V3_S0_MCP_PLL_UF (24)
- =PP3V3_S0_MCP_VPLL_UF (25)
- =PP3V3_S0_MCP_DAC_UF (25)
- =PP3V3_S0_MCP (21, 22, 24)
- =PP3V3_S0_AUDIO (54, 58, 59)
- =PP3V3_S0_ODD (39)
- =PP3V3_S0_VMON (68)
- =PP3V3_S0_SMBUS_MCP_1 (45)
- =PP3V3_FC_CON (32)
- =PP3V3_S0_EXCARD (32)
- =PP3V3_S0_LVDSDDCMUX (80)
- =PP3V3_S0_BATTCHARGERTMPSNSR (48)
- =PP3V3_GPU_SMBUS_SMC_0_S0 (45)
- =PP3V3_S0_TPAD (51)

=PP2V5_S0_REG (86) → PP2V5_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE

- =PP2V5_S0_GMUX (83)

=PP1V2_S0_REG (86) → PP1V2_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE

- =PP1V2_S0_GMUX (83)

## 1.8V/DDR 1.5V Rails

=PP1V8_S0_REG (67) → PP1V8_S0 (7)
500 mA max supply
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- 190 mA =PP3V3R1V8_S0_MCP_IFP_VDD (18, 25)

=PPDDR_S3_REG (64) → PP1V8R1V5_S3 (7)
MIN_LINE_WIDTH=0.8 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V8R1V5_S0_MCP_FET (69)
- =PPVIN_S0_DDRREG_LDO (64)
- =PP1V5_S3_MEM_A (28)
- =PP1V5_S3_MEM_B (29)
- =PP1V5_S3_MEMRESET (30)

=PP1V8R1V5_S0_FET (69) → PP1V8R1V5_S0_FET (7)
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

- 4771 mA =PPMCPDDR_ISNS_R (47)
- 130 mA =PP1V5_S0_CPU (11, 12)
- 500 mA =PP1V5_S0_EXCARD (32)
- =PP1V5_S0_VMON (68)
- =PP1V5_FC_CON (32)

(24, 16) =PP1V8R1V5_S0_MCP_MEM → PPMCPDDR_ISNS (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S0_MEM_A (28)
- =PP1V5_S0_MEM_B (29)
- =PPMCPDDR_ISNS (47)

=PP1V05_S0_FET (69) → PP1V05_S0_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- 1034 mA =PP1V05_S0_MCP_AVDD_UF (24)
- =PP1V05_S0_MCP_PEX_DVDD (8, 24)
- =PP1V05_S0_MCP_PLL_UF (24)
- =PP1V05_S0_MCP_SATA_DVDD (8, 24)
- =PP1V05_S0_MCP_HDMI_VDD (18, 25)
- =PP1V05_S0_VMON (68)

(24, 8) =PP1V05_S0_MCP_PEX_DVDD → =PP1V05_S0_MCP_PEX_DVDD0 (17); =PP1V05_S0_MCP_PEX_DVDD1 (17)

(24) PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE) → =PP1V05_S0_MCP_PEX_AVDD0 (17); =PP1V05_S0_MCP_PEX_AVDD1 (17)

(24, 8) =PP1V05_S0_MCP_SATA_DVDD → =PP1V05_S0_MCP_SATA_DVDD0 (20)

(24) PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE) → =PP1V05_S0_MCP_SATA_AVDD0 (20)

=PP1V05_S5_MCP (67) → PP1V2R1V05_S5 (1.1V for A01) (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

241 mA max load

- 105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC (22, 24)
- 139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET (34)
- =PP1V05_S5_P1V05S0FET (69)

=PPCPUVTT_S0_REG (66) → PPCPUVTT_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

5300 mA

- 4500 mA =PP1V05_S0_CPU (6, 10, 11, 12, 13, 62)
- =PP1V05_S0_SMC_LS (43)
- 1182 mA =PP1V05_S0_MCP_FSB (9, 14, 22, 24)

(64, 27) =PPVTT_S3_DDR_BUF → PPVTTDDR_S3 (7)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO (64) → PP0V9R0V75_S0_DDRVTT (7)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

- =PP0V75_S0_MEM_VTT_A (28)
- =PP0V75_S0_MEM_VTT_B (29)
- =PPVTT_S0_VTTCLAMP (69)

OR 0.75V

## ENET Rails

=PP1V05_ENET_FET (34) → PP1V2R1V05_ENET (7)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_ENET_MCP_PLL_MAC (24)
- =PP1V05_ENET_MCP_RMGT (18, 24)
- =PP1V05_ENET_PHY (33)

=PP3V3_ENET_FET (34) → PP3V3_ENET_PHY (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

- =PP3V3_ENET_MCP_RMGT (18, 24)
- =PP3V3_ENET_PHY (33)

## "FW" (FireWire) Rails

=PPBUS_S5_FW_FET (37) → PPVP_FW (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

- =PPVP_FW_PORT1 (38)
- =PPVP_FW_PHY_CPS_FET (38)

=PP1V0_FW_REG (67) → PP1V0_FW (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V0_FW_FWPHY (36)

## "GPU" Rails

=PP3V3_S0GPU_FET (69) → PP3V3_S0GPU (7)
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_GPU_VDD33 (6, 75, 76)
- =PP3V3_GPU_MIO (75, 76)
- =PP3V3_GPU_LVDS_DDC (80)
- =PP3V3_GPU_PWRCTL (68)
- =PP3V3_GPU_VCORELOGIC (78)
- =PP3V3_GPU_P1V8S0 (67)

=PP1V1_S0GPU_REG (82) → PP1V1_S0GPU_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE

- =PP1V1_GPU_PEX_IOVDDQ (70)
- =PP1V1_GPU_PEX_IOVDD (70)
- =PP1V1_GPU_PEX_PLLXVDD (70)
- =PP1V1_GPU_PLLVDD (75)
- =PP1V1_GPU_H_PLLVDD (75)
- =PP1V1_GPU_VID_PLLVDD (75)
- =PP1V1_GPU_FBPLLAVDD (72)
- =PP1V1_GPU_IFPCD_IOVDD (77)

=PP1V8_GPUIFPX_REG (67) → PP1V8_GPUIFPX (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_GPU_IFPX (77)

=PP1V8_S0GPU_ISNS (47) → PP1V8_S0GPU_ISNS (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_GPU_FB_VDD (73, 74)
- =PP1V8_GPU_FB_VDDQ (9, 73, 74)
- =PP1V8_GPU_FBVDDQ (71)
- =PP1V8_GPU_FBIO (72)

=PPVCORE_GPU_REG (78, 46) → PPVCORE_GPU (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.4V
MAKE_BASE=TRUE

- =PPVCORE_GPU (71)

=PP1V8_GPU_REG (82) → PP1V8_S0GPU_ISNS_R (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.45V
MAKE_BASE=TRUE

- =PP1V8_S0GPU_ISNS_R (47)

## Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)


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## Thermal Module Holes

ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
Bottom Left GPU TM Hole
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

## Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0950 TH — GND_CHASSIS_FAN (SL-3.1X2.7-6CIR-NSP)
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0990 3R2P5 — GND_CHASSIS_BATTCONN

=PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98

## Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

=PP1V05_S0_MCP_FSB
NO STUFF R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0990 150 1% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402

CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

## Bosses for VRAM HS

NO STUFF ZT0951 4.0OD1.65H-M1.6X0.35
NO STUFF ZT0952 4.0OD1.65H-M1.6X0.35
NO STUFF ZT0953 4.0OD1.65H-M1.6X0.35

ZT0931 STDOFF-4.0OD3.0H-TH VENICE
ZT0934 STDOFF-4.0OD3.0H-TH
ZT0932 STDOFF-4.0OD3.0H-TH VENICE
ZT0935 STDOFF-4.0OD3.0H-TH
ZT0933 STDOFF-4.0OD3.0H-TH VENICE

NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>
NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
(MAKE_BASE=TRUE, NO_TEST=TRUE)

TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM

ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3>
NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>
(MAKE_BASE=TRUE)

### CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L
CPU_VID<0..6> — IMVP6_VID<0..6>
CPU_BSEL<0..2> — =MCP_BSEL<0..2>
MEM_VTT_EN — =DDRVTT_EN
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB

### GPU signals

PEG_D2R_P<0..15> — =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15>

PCIE_CLK100M_FC_P — TP_PCIE_CLK100M_PE4P
PCIE_CLK100M_FC_N — TP_PCIE_CLK100M_PE4N
PCIE_FC_R2D_C_P — TP_PCIE_PE4_R2D_CP
PCIE_FC_R2D_C_N — TP_PCIE_PE4_R2D_CN
FC_CLKREQ_L — TP_PE4_CLKREQ_L
FC_PRSNT_L — TP_PE4_PRSNT_L
PCIE_FC_D2R_P — TP_PCIE_PE4_D2RP
PCIE_FC_D2R_N — TP_PCIE_PE4_D2RN

### GMUX ALIASES

LCD_BKLT_EN — LVDS_BKL_ON
DP_IG_ML_P<3> — =MCP_HDMI_TXC_P
DP_IG_ML_N<3> — =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK
DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA
DP_IG_HPD — =MCP_HDMI_HPD
PM_ALL_GPU_PGOOD — ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG
EG_RESET_L — GPU_RESET_L

JTAG_GMUX_TDI — GMUX_JTAG_TDI
JTAG_GMUX_TMS — GMUX_JTAG_TMS
JTAG_GMUX_TDO — GMUX_JTAG_TDO
LVDS_IG_BKL_ON — IG_BKLT_EN
LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN

TP_USB_EXTDP — USB_EXTD_P
TP_USB_EXTDN — USB_EXTD_N
TP_USB_MINIP — USB_MINI_P
TP_USB_MININ — USB_MINI_N
GMUX_INT — =DVI_HPD_GMUX_INT

R0903 0 5% 1/16W MF-LF 402
MCP_SPKR — SMC_MCP_SAFE_MODE

TP_MEM_A_A<15> — MEM_A_A<15>
TP_MEM_B_A<15> — MEM_B_A<15>
TP_USB_EXTCP — USB_EXTC_P
TP_USB_EXTCN — USB_EXTC_N
TP_CPU_PECI_MCP — CPU_PECI_MCP
TP_MCP_GPIO_17 — AUD_IP_PERIPHERAL_DET
PCIE_RESET_L — FC_RESET_L

### AUDIO ALIASES

HDA_BITCLK — HDA_BIT_CLK
XW0900
=PP5V_S3_AUDIO_PWR — PP5V_S3_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
XW0901 — PP5V_S3_AUDIO_AMP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
R0902 10K 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN

### ETHERNET ALIASES

=P3V3ENET_EN — PM_SLP_RMGT_L
=P1V05ENET_EN
=PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
=RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG

## MCP79 PCIe PRSNT# Straps

These need work. Add other PRSNT# straps if needed. .

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L
R0927 0 5% 1/16W MF-LF 402 — NO STUFF
PEG_PRSNT_L
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L

MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER
=MCP_MII_CRS
=MCP_MII_COL

=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD1

## Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.09MM, VOLTAGE=0V)

## Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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U1000
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1 OF 4

ADDR GROUP0
FSB_A_L<3> J4
FSB_A_L<4> L5
FSB_A_L<5> L4
FSB_A_L<6> K5
FSB_A_L<7> M3
FSB_A_L<8> N2
FSB_A_L<9> J1
FSB_A_L<10> N3
FSB_A_L<11> P5
FSB_A_L<12> P2
FSB_A_L<13> L2
FSB_A_L<14> P4
FSB_A_L<15> P1
FSB_A_L<16> R1
FSB_ADSTB_L<0> M1

ADDR GROUP1
FSB_A_L<17> Y2
FSB_A_L<18> U5
FSB_A_L<19> R3
FSB_A_L<20> W6
FSB_A_L<21> U4
FSB_A_L<22> Y5
FSB_A_L<23> U1
FSB_A_L<24> R4
FSB_A_L<25> T5
FSB_A_L<26> T3
FSB_A_L<27> W2
FSB_A_L<28> W5
FSB_A_L<29> Y4
FSB_A_L<30> U2
FSB_A_L<31> V4
FSB_A_L<32> W3
FSB_A_L<33> AA4
FSB_A_L<34> AB2
FSB_A_L<35> AA3
FSB_ADSTB_L<1> V1

ICH
CPU_A20M_L A6
CPU_FERR_L A5
CPU_IGNNE_L C4
CPU_STPCLK_L D5
CPU_INTR C6
CPU_NMI B4
CPU_SMI_L A3

RESERVED
TP_CPU_RSVD0 M4
TP_CPU_RSVD1 N5
TP_CPU_RSVD2 T2
TP_CPU_RSVD3 V3
TP_CPU_RSVD4 B2
TP_CPU_RSVD5 F6
TP_CPU_RSVD6 D2
TP_CPU_RSVD7 D22
TP_CPU_RSVD8 D3

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

=PP1V05_S0_CPU
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

=PP1V05_S0_CPU
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

0.5" MAX LENGTH FOR CPU_GTLREF
CPU_GTLREF AD26
CPU_TEST1 C23
CPU_TEST2 D25
TP_CPU_TEST3 C24
CPU_TEST4 AF26
TP_CPU_TEST5 AF1
TP_CPU_TEST6 A26
TP_CPU_TEST7 C3
CPU_BSEL<0> B22
CPU_BSEL<1> B23
CPU_BSEL<2> C21

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

R1020 54.9 1% 1/16W MF-LF 402 =PP1V05_S0_CPU
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
XDP_TMS
XDP_TDI
XDP_TDO
XDP_TCK
XDP_TRST_L
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
FSB_D_L<0> E22
FSB_D_L<1> F24
FSB_D_L<2> E26
FSB_D_L<3> G22
FSB_D_L<4> F23
FSB_D_L<5> G25
FSB_D_L<6> E25
FSB_D_L<7> E23
FSB_D_L<8> K24
FSB_D_L<9> G24
FSB_D_L<10> J24
FSB_D_L<11> J23
FSB_D_L<12> H22
FSB_D_L<13> F26
FSB_D_L<14> K22
FSB_D_L<15> H23
FSB_DSTB_L_N<0> J26
FSB_DSTB_L_P<0> H26
FSB_DINV_L<0> H25

DATA GRP 1
FSB_D_L<16> N22
FSB_D_L<17> K25
FSB_D_L<18> P26
FSB_D_L<19> R23
FSB_D_L<20> L23
FSB_D_L<21> M24
FSB_D_L<22> L22
FSB_D_L<23> M23
FSB_D_L<24> P25
FSB_D_L<25> P23
FSB_D_L<26> P22
FSB_D_L<27> T24
FSB_D_L<28> R24
FSB_D_L<29> L25
FSB_D_L<30> T25
FSB_D_L<31> N25
FSB_DSTB_L_N<1> L26
FSB_DSTB_L_P<1> M26
FSB_DINV_L<1> N24

DATA GRP 2
FSB_D_L<32> Y22
FSB_D_L<33> AB24
FSB_D_L<34> V24
FSB_D_L<35> V26
FSB_D_L<36> V23
FSB_D_L<37> T22
FSB_D_L<38> U25
FSB_D_L<39> U23
FSB_D_L<40> Y25
FSB_D_L<41> W22
FSB_D_L<42> Y23
FSB_D_L<43> W24
FSB_D_L<44> W25
FSB_D_L<45> AA23
FSB_D_L<46> AA24
FSB_D_L<47> AB25
FSB_DSTB_L_N<2> Y26
FSB_DSTB_L_P<2> AA26
FSB_DINV_L<2> U22

DATA GRP 3
FSB_D_L<48> AE24
FSB_D_L<49> AD24
FSB_D_L<50> AA21
FSB_D_L<51> AB22
FSB_D_L<52> AB21
FSB_D_L<53> AC26
FSB_D_L<54> AD20
FSB_D_L<55> AE22
FSB_D_L<56> AF23
FSB_D_L<57> AC25
FSB_D_L<58> AE21
FSB_D_L<59> AD21
FSB_D_L<60> AC22
FSB_D_L<61> AD23
FSB_D_L<62> AF22
FSB_D_L<63> AC23
FSB_DSTB_L_N<3> AE25
FSB_DSTB_L_P<3> AF24
FSB_DINV_L<3> AC20

MISC
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

# CPU FSB

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007


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| SCALE: NONE | SHT 10 OF 109 | |

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(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 46

| Standard Voltage: | Low Voltage: | Ultra Low Voltage: |
|---|---|---|
| 44.0 A (Design Target) | 23.0 A (Design Target) | 17.0 A (Design Target) |
| 41.0 A (HFM) | 21.0 A (HFM) | TBD A (HFM) |
| 30.4 A (LFM) | 18.7 A (LFM) | TBD A (LFM) |
| 25.5 A (SuperLFM) | TBD A (SuperLFM) | |
| 27.4 A (Auto-Halt/Stop-Grant HFM) | TBD A (Auto-Halt/Stop-Grant HFM) | TBD A (Auto-Halt/Stop-Grant HFM) |
| 17.0 A (Auto-Halt/Stop-Grant SuperLFM) | TBD A (Auto-Halt/Stop-Grant SuperLFM) | TBD A (Auto-Halt/Stop-Grant LFM) |
| 27.4 A (Sleep HFM) | TBD A (Sleep HFM) | TBD A (Sleep HFM) |
| 16.8 A (Sleep SuperLFM) | TBD A (Sleep SuperLFM) | TBD A (Sleep LFM) |
| 25.0 A (Deep Sleep HFM) | TBD A (Deep Sleep HFM) | TBD A (Deep Sleep HFM) |
| 16.0 A (Deep Sleep SuperLFM) | TBD A (Deep Sleep SuperLFM) | TBD A (Deep Sleep LFM) |
| 11.5 A (Deeper Sleep) | TBD A (Deeper Sleep) | TBD A (Deeper Sleep) |
| 9.4 A (Enhanced Deeper Sleep) | TBD A (Enhanced Deeper Sleep) | TBD A (Enhanced Deeper Sleep) |

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VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 6 8 10 12 13 62

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

| | | | |
|---|---|---|---|
| VID0 | AD6 | CPU_VID<0> | OUT 9 87 |
| VID1 | AF5 | CPU_VID<1> | OUT 9 87 |
| VID2 | AE5 | CPU_VID<2> | OUT 9 87 |
| VID3 | AF4 | CPU_VID<3> | OUT 9 87 |
| VID4 | AE3 | CPU_VID<4> | OUT 9 87 |
| VID5 | AF3 | CPU_VID<5> | OUT 9 87 |
| VID6 | AE2 | CPU_VID<6> | OUT 9 87 |
| VCCSENSE | AF7 | CPU_VCCSENSE_P | OUT 62 87 |
| VSSSENSE | AE7 | CPU_VCCSENSE_N | OUT 62 87 |

=PPVCORE_S0_CPU 8 11 12 46

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
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VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

# CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007


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Current numbers from Merom for Santa Rosa EMTS, doc #22221.

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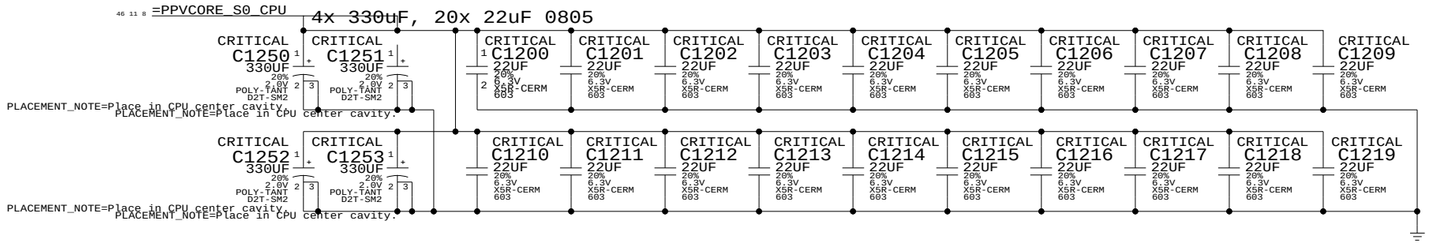
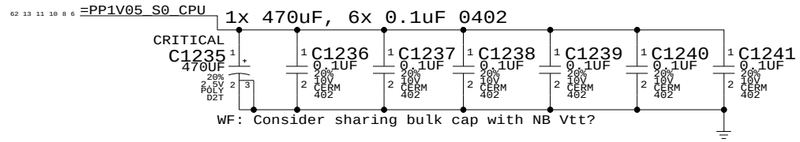
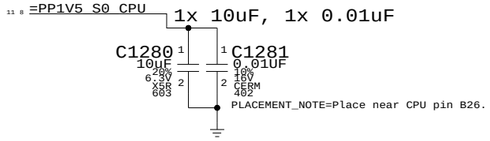
## CPU VCORE HF AND BULK DECOUPLING


46 11 8 =PPVCORE_S0_CPU
4x 330uF, 20x 22uF 0805
CRITICAL C1250 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1251 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1252 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1253 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C1200 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1201 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1202 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1203 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1204 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1205 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1206 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1207 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1208 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1209 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1210 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1211 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1212 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1213 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1214 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1215 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1216 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1217 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1218 22UF 20% 6.3V X5R-CERM 603
CRITICAL C1219 22UF 20% 6.3V X5R-CERM 603
PLACEMENT_NOTE=Place in CPU center cavity.
PLACEMENT_NOTE=Place in CPU center cavity.

## VCCP (CPU I/O) DECOUPLING


62 13 11 10 8 6 =PP1V05_S0_CPU
1x 470uF, 6x 0.1uF 0402
CRITICAL C1235 470UF 20% 2.5V POLY-TANT D2T
C1236 0.1UF 20% 10V CERM 402
C1237 0.1UF 20% 10V CERM 402
C1238 0.1UF 20% 10V CERM 402
C1239 0.1UF 20% 10V CERM 402
C1240 0.1UF 20% 10V CERM 402
C1241 0.1UF 20% 10V CERM 402
WF: Consider sharing bulk cap with NB Vtt?

## VCCA (CPU AVdd) DECOUPLING




# CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007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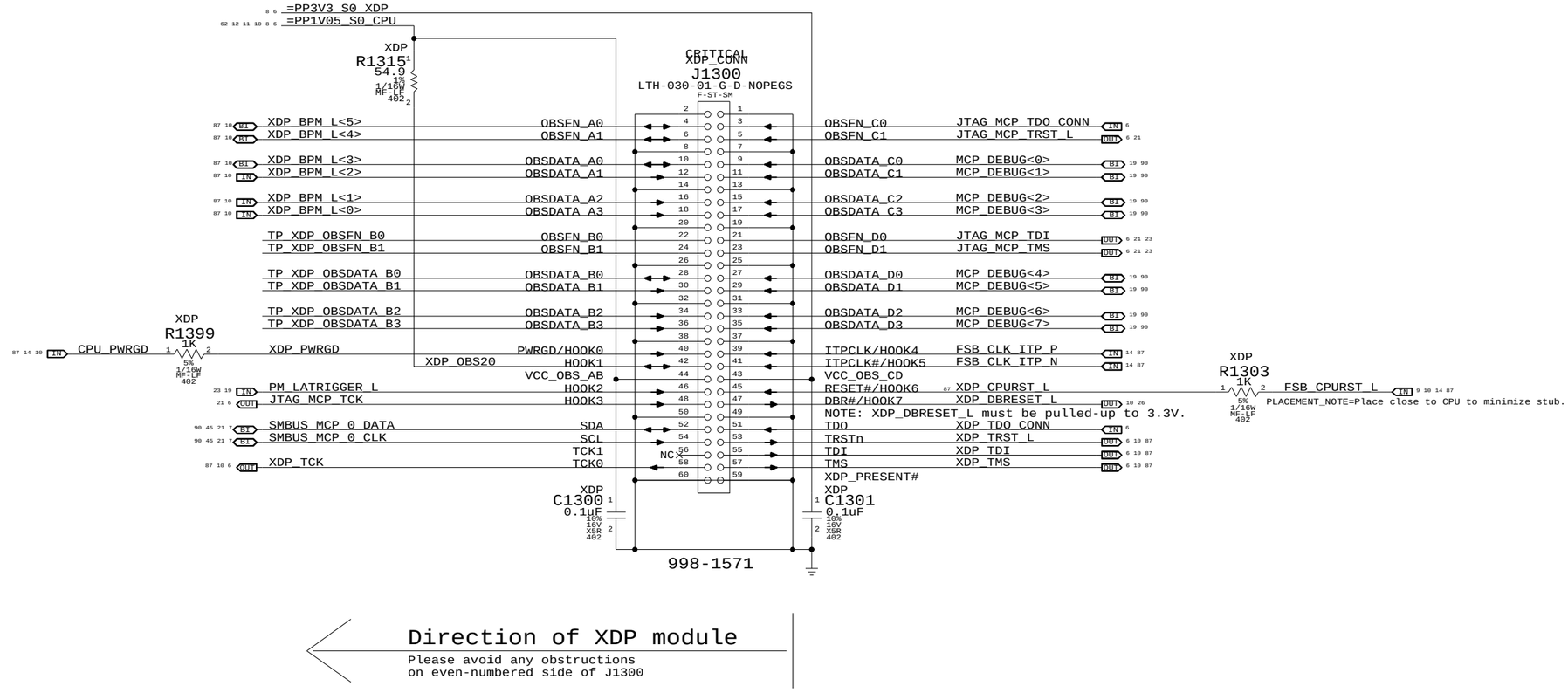
# Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

## MCP79-specific pinout




Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008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|---|---|---|
| NONE | 13 | 109 |

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OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

| | | | |
|---|---|---|---|
| FSB_DSTB_L_P<0> | T40 | CPU_DSTBP0# | |
| FSB_DSTB_L_N<0> | U40 | CPU_DSTBN0# | |
| FSB_DINV_L<0> | V41 | CPU_DBI0# | |
| FSB_DSTB_L_P<1> | W39 | CPU_DSTBP1# | |
| FSB_DSTB_L_N<1> | W37 | CPU_DSTBN1# | |
| FSB_DINV_L<1> | V35 | CPU_DBI1# | |
| FSB_DSTB_L_P<2> | N37 | CPU_DSTBP2# | |
| FSB_DSTB_L_N<2> | L36 | CPU_DSTBN2# | |
| FSB_DINV_L<2> | N35 | CPU_DBI2# | |
| FSB_DSTB_L_P<3> | M39 | CPU_DSTBP3# | |
| FSB_DSTB_L_N<3> | M41 | CPU_DSTBN3# | |
| FSB_DINV_L<3> | J41 | CPU_DBI3# | |
| FSB_A_L<3> | AC34 | CPU_A3# | |
| FSB_A_L<4> | AE38 | CPU_A4# | |
| FSB_A_L<5> | AE34 | CPU_A5# | |
| FSB_A_L<6> | AC37 | CPU_A6# | |
| FSB_A_L<7> | AE37 | CPU_A7# | |
| FSB_A_L<8> | AE35 | CPU_A8# | |
| FSB_A_L<9> | AB35 | CPU_A9# | |
| FSB_A_L<10> | AF35 | CPU_A10# | |
| FSB_A_L<11> | AG35 | CPU_A11# | |
| FSB_A_L<12> | AG39 | CPU_A12# | |
| FSB_A_L<13> | AE33 | CPU_A13# | |
| FSB_A_L<14> | AG37 | CPU_A14# | |
| FSB_A_L<15> | AG38 | CPU_A15# | |
| FSB_A_L<16> | AG34 | CPU_A16# | |
| FSB_A_L<17> | AN38 | CPU_A17# | |
| FSB_A_L<18> | AL39 | CPU_A18# | |
| FSB_A_L<19> | AG33 | CPU_A19# | |
| FSB_A_L<20> | AL33 | CPU_A20# | |
| FSB_A_L<21> | AJ33 | CPU_A21# | |
| FSB_A_L<22> | AN36 | CPU_A22# | |
| FSB_A_L<23> | AJ35 | CPU_A23# | |
| FSB_A_L<24> | AJ37 | CPU_A24# | |
| FSB_A_L<25> | AJ36 | CPU_A25# | |
| FSB_A_L<26> | AJ38 | CPU_A26# | |
| FSB_A_L<27> | AL37 | CPU_A27# | |
| FSB_A_L<28> | AL34 | CPU_A28# | |
| FSB_A_L<29> | AN37 | CPU_A29# | |
| FSB_A_L<30> | AJ34 | CPU_A30# | |
| FSB_A_L<31> | AL38 | CPU_A31# | |
| FSB_A_L<32> | AL35 | CPU_A32# | |
| FSB_A_L<33> | AN34 | CPU_A33# | |
| FSB_A_L<34> | AR39 | CPU_A34# | |
| FSB_A_L<35> | AN35 | CPU_A35# | |
| FSB_ADSTB_L<0> | AE36 | CPU_ADSTB0# | |
| FSB_ADSTB_L<1> | AK35 | CPU_ADSTB1# | |
| FSB_REQ_L<0> | AC38 | CPU_REQ0# | |
| FSB_REQ_L<1> | AA33 | CPU_REQ1# | |
| FSB_REQ_L<2> | AC39 | CPU_REQ2# | |
| FSB_REQ_L<3> | AC33 | CPU_REQ3# | |
| FSB_REQ_L<4> | AC35 | CPU_REQ4# | |
| FSB_ADS_L | AD42 | CPU_ADS# | |
| FSB_BNR_L | AD43 | CPU_BNR# | |
| FSB_BREQ0_L | AE40 | CPU_BR0# | |
| FSB_BREQ1_L | AL32 | CPU_BR1# | |
| FSB_DBSY_L | AD39 | CPU_DBSY# | |
| FSB_DRDY_L | AD41 | CPU_DRDY# | |
| FSB_HIT_L | AB42 | CPU_HIT# | |
| FSB_HITM_L | AD40 | CPU_HITM# | |
| FSB_LOCK_L | AC43 | CPU_LOCK# | |
| FSB_TRDY_L | AE41 | CPU_TRDY# | |
| CPU_PECI_MCP | E41 | CPU_PECI | |
| CPU_PROCHOT_L | AJ41 | CPU_PROCHOT# | |
| | AG43 | CPU_THERMTRIP# | |
| | AH40 | CPU_FERR# | |
| (MCP_BSEL<2>) | F42 | CPU_BSEL2 | |
| (MCP_BSEL<1>) | D42 | CPU_BSEL1 | |
| (MCP_BSEL<0>) | F41 | CPU_BSEL0 | |
| FSB_RS_L<0> | AC41 | CPU_RS0# | |
| FSB_RS_L<1> | AB41 | CPU_RS1# | |
| FSB_RS_L<2> | AC42 | CPU_RS2# | |
| PP1V05_S0_MCP_PLL_FSB | | | |
| 270 mA (A01) | 206 mA | AG27 | +V_DLL_DLCELL_AVDD |
| | 20 mA | AH27 | +V_PLL_MCLK |
| | 29 mA | AG28 | +V_PLL_FSB |
| | 15 mA | AH28 | +V_PLL_CPU |
| MCP_BCLK_VML_COMP_VDD | AM39 | BCLK_VML_COMP_VDD | |
| MCP_BCLK_VML_COMP_GND | AM40 | BCLK_VML_COMP_GND | |
| MCP_CPU_COMP_VCC | AM43 | CPU_COMP_VCC | |
| MCP_CPU_COMP_GND | AM42 | CPU_COMP_GND | |

| | | | |
|---|---|---|---|
| CPU_D0# | Y43 | FSB_D_L<0> | |
| CPU_D1# | W42 | FSB_D_L<1> | |
| CPU_D2# | Y40 | FSB_D_L<2> | |
| CPU_D3# | W41 | FSB_D_L<3> | |
| CPU_D4# | Y39 | FSB_D_L<4> | |
| CPU_D5# | V42 | FSB_D_L<5> | |
| CPU_D6# | Y41 | FSB_D_L<6> | |
| CPU_D7# | Y42 | FSB_D_L<7> | |
| CPU_D8# | P42 | FSB_D_L<8> | |
| CPU_D9# | U41 | FSB_D_L<9> | |
| CPU_D10# | R42 | FSB_D_L<10> | |
| CPU_D11# | T39 | FSB_D_L<11> | |
| CPU_D12# | T42 | FSB_D_L<12> | |
| CPU_D13# | T41 | FSB_D_L<13> | |
| CPU_D14# | R41 | FSB_D_L<14> | |
| CPU_D15# | T43 | FSB_D_L<15> | |
| CPU_D16# | W35 | FSB_D_L<16> | |
| CPU_D17# | AA37 | FSB_D_L<17> | |
| CPU_D18# | W33 | FSB_D_L<18> | |
| CPU_D19# | W34 | FSB_D_L<19> | |
| CPU_D20# | AA36 | FSB_D_L<20> | |
| CPU_D21# | AA34 | FSB_D_L<21> | |
| CPU_D22# | AA38 | FSB_D_L<22> | |
| CPU_D23# | AA35 | FSB_D_L<23> | |
| CPU_D24# | U38 | FSB_D_L<24> | |
| CPU_D25# | U36 | FSB_D_L<25> | |
| CPU_D26# | U35 | FSB_D_L<26> | |
| CPU_D27# | U33 | FSB_D_L<27> | |
| CPU_D28# | U34 | FSB_D_L<28> | |
| CPU_D29# | W38 | FSB_D_L<29> | |
| CPU_D30# | R33 | FSB_D_L<30> | |
| CPU_D31# | U37 | FSB_D_L<31> | |
| CPU_D32# | N34 | FSB_D_L<32> | |
| CPU_D33# | N33 | FSB_D_L<33> | |
| CPU_D34# | R34 | FSB_D_L<34> | |
| CPU_D35# | R35 | FSB_D_L<35> | |
| CPU_D36# | P35 | FSB_D_L<36> | |
| CPU_D37# | R39 | FSB_D_L<37> | |
| CPU_D38# | R37 | FSB_D_L<38> | |
| CPU_D39# | R38 | FSB_D_L<39> | |
| CPU_D40# | L37 | FSB_D_L<40> | |
| CPU_D41# | L39 | FSB_D_L<41> | |
| CPU_D42# | L38 | FSB_D_L<42> | |
| CPU_D43# | N36 | FSB_D_L<43> | |
| CPU_D44# | N38 | FSB_D_L<44> | |
| CPU_D45# | J39 | FSB_D_L<45> | |
| CPU_D46# | J38 | FSB_D_L<46> | |
| CPU_D47# | J37 | FSB_D_L<47> | |
| CPU_D48# | L42 | FSB_D_L<48> | |
| CPU_D49# | M42 | FSB_D_L<49> | |
| CPU_D50# | P41 | FSB_D_L<50> | |
| CPU_D51# | N41 | FSB_D_L<51> | |
| CPU_D52# | N40 | FSB_D_L<52> | |
| CPU_D53# | M40 | FSB_D_L<53> | |
| CPU_D54# | H40 | FSB_D_L<54> | |
| CPU_D55# | K42 | FSB_D_L<55> | |
| CPU_D56# | H41 | FSB_D_L<56> | |
| CPU_D57# | L41 | FSB_D_L<57> | |
| CPU_D58# | H43 | FSB_D_L<58> | |
| CPU_D59# | H42 | FSB_D_L<59> | |
| CPU_D60# | K41 | FSB_D_L<60> | |
| CPU_D61# | J40 | FSB_D_L<61> | |
| CPU_D62# | H39 | FSB_D_L<62> | |
| CPU_D63# | M43 | FSB_D_L<63> | |
| CPU_BPRI# | AA41 | FSB_BPRI_L | |
| CPU_DEFER# | AA40 | FSB_DEFER_L | |
| BCLK_OUT_CPU_P | G42 | FSB_CLK_CPU_P | |
| BCLK_OUT_CPU_N | G41 | FSB_CLK_CPU_N | |
| BCLK_OUT_ITP_P | AL43 | FSB_CLK_ITP_P | |
| BCLK_OUT_ITP_N | AL42 | FSB_CLK_ITP_N | |
| BCLK_OUT_NB_P | AL41 | FSB_CLK_MCP_P | |
| BCLK_OUT_NB_N | AK42 | FSB_CLK_MCP_N | |
| BCLK_IN_N | AK41 | | |
| BCLK_IN_P | AJ40 | | |
| CPU_A20M# | AF41 | CPU_A20M_L | |
| CPU_IGNNE# | AH39 | CPU_IGNNE_L | |
| CPU_INIT# | AH42 | CPU_INIT_L | |
| CPU_INTR | AF42 | CPU_INTR | |
| CPU_NMI | AG41 | CPU_NMI | |
| CPU_SMI# | AH41 | CPU_SMI_L | |
| CPU_PWRGD | AH43 | CPU_PWRGD | |
| CPU_RESET# | H38 | FSB_CPURST_L | |
| CPU_SLP# | AM33 | FSB_CPUSLP_L | |
| CPU_DPSLP# | AN33 | CPU_DPSLP_L | |
| CPU_DPWR# | AM32 | FSB_DPWR_L | |
| CPU_STPCLK# | AG42 | CPU_STPCLK_L | |
| CPU_DPRSTP# | AN32 | CPU_DPRSTP_L | |

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/10W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/10W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/10W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

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# MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


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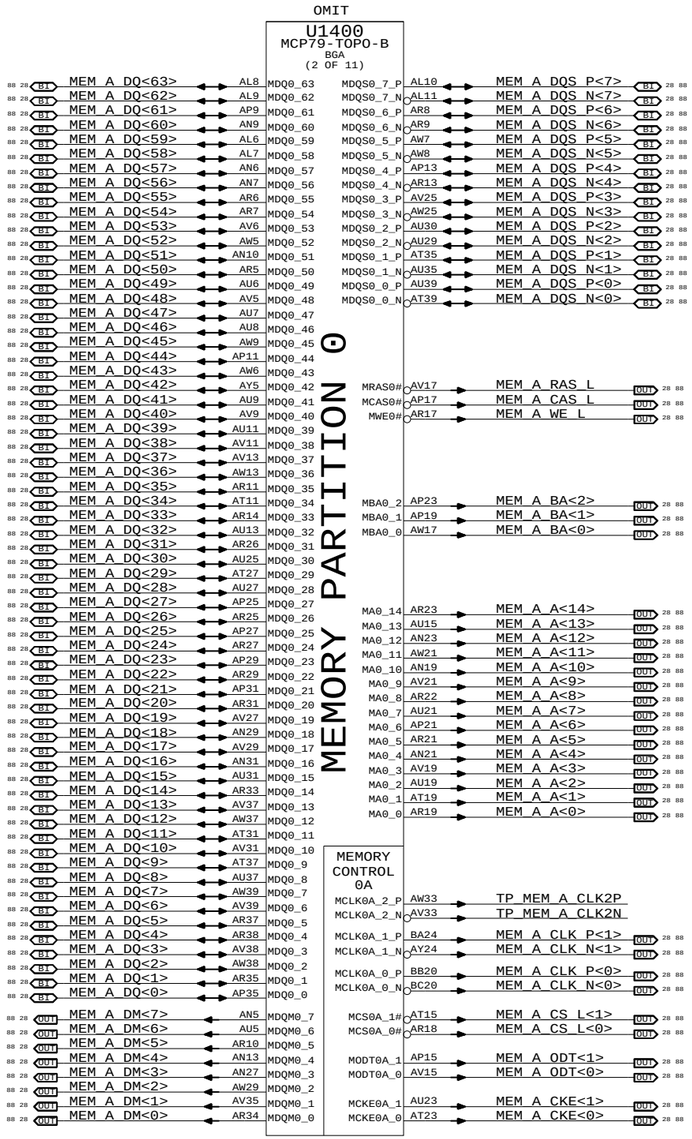


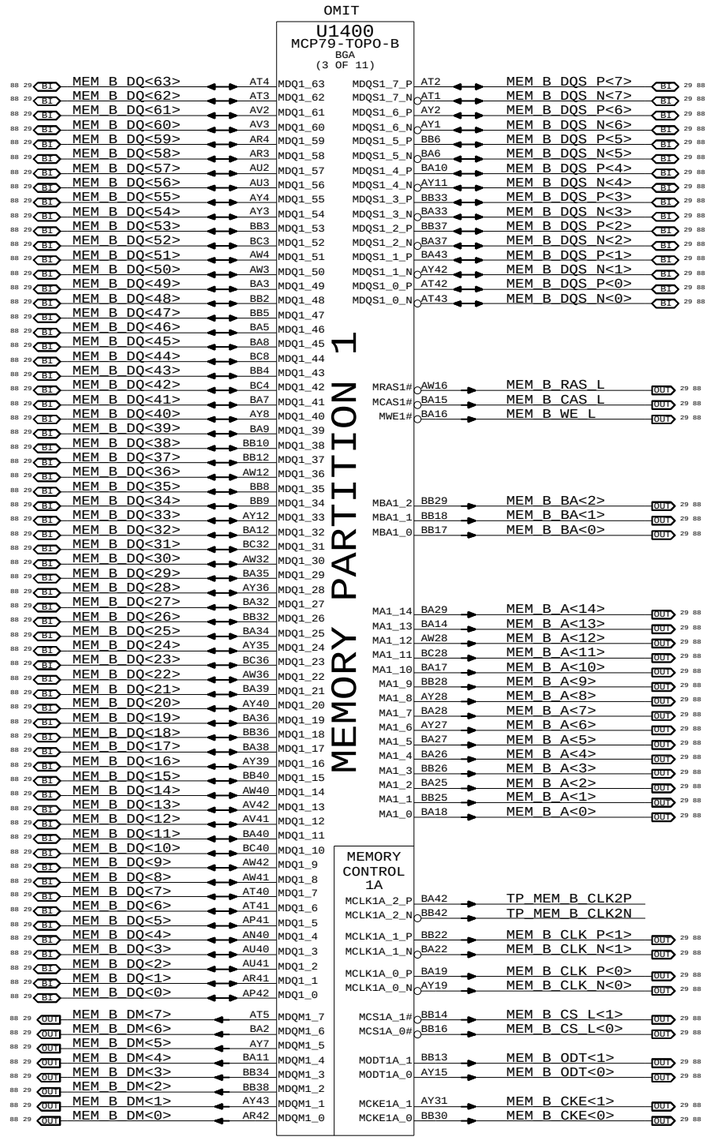


# MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

| | | |
|---|---|---|
| TP_MEM_A_CLK5P | AU33 | MCLK0B_2_P |
| TP_MEM_A_CLK5N | AU34 | MCLK0B_2_N |
| TP_MEM_A_CLK4P | BB24 | MCLK0B_1_P |
| TP_MEM_A_CLK4N | BC24 | MCLK0B_1_N |
| TP_MEM_A_CLK3P | BA21 | MCLK0B_0_P |
| TP_MEM_A_CLK3N | BB21 | MCLK0B_0_N |
| TP_MEM_A_CS_L<2> | AU17 | MCS0B_0# |
| TP_MEM_A_CS_L<3> | AR15 | MCS0B_1# |
| TP_MEM_A_ODT<2> | AN17 | MODT0B_0 |
| TP_MEM_A_ODT<3> | AN15 | MODT0B_1 |
| TP_MEM_A_CKE<2> | AV23 | MCKE0B_0 |
| TP_MEM_A_CKE<3> | AN25 | MCKE0B_1 |

MEMORY CONTROL 1B

| | | |
|---|---|---|
| MCLK1B_2_P | BA41 | TP_MEM_B_CLK5P |
| MCLK1B_2_N | BB41 | TP_MEM_B_CLK5N |
| MCLK1B_1_P | AY23 | TP_MEM_B_CLK4P |
| MCLK1B_1_N | BA23 | TP_MEM_B_CLK4N |
| MCLK1B_0_P | BA20 | TP_MEM_B_CLK3P |
| MCLK1B_0_N | AY20 | TP_MEM_B_CLK3N |
| MCS1B_0# | BC16 | TP_MEM_B_CS_L<2> |
| MCS1B_1# | BA13 | TP_MEM_B_CS_L<3> |
| MODT1B_0 | AY16 | TP_MEM_B_ODT<2> |
| MODT1B_1 | BC13 | TP_MEM_B_ODT<3> |
| MCKE1B_0 | BA30 | TP_MEM_B_CKE<2> |
| MCKE1B_1 | BA31 | TP_MEM_B_CKE<3> |

=PP1V8R1V5_S0_MCP_MEM (24 16 8)

R1610[1] 40.2 1% 1/16W MF-LF 402 (2)

R1611[1] 40.2 1% 1/16W MF-LF 402 (2)

PP1V05_S0_MCP_PLL_CORE (24)
87 mA (A01)

| | | |
|---|---|---|
| 17 mA | T27 | +V_PLL_XREF_XS |
| 12 mA | U28 | +V_PLL_DP |
| 19 mA | U27 | +V_PLL_CORE |
| 39 mA | T28 | +V_VPLL |

MCP_MEM_COMP_VDD (88) AN41 MEM_COMP_VDD
MCP_MEM_COMP_GND (88) AM41 MEM_COMP_GND

MRESET0# AY32 → MCP_MEM_RESET_L (OUT 30)
TP or NC for DDR2.

=PP1V8R1V5_S0_MCP_MEM (8 16 24)
4771 mA (A01, DDR3)

| | | |
|---|---|---|
| +VDD_MEM1 | AM17 | GND1 AA22 |
| +VDD_MEM2 | AM19 | GND2 AP12 |
| +VDD_MEM3 | AM21 | GND3 G30 |
| +VDD_MEM4 | AM23 | GND4 P10 |
| +VDD_MEM5 | AM25 | GND5 T10 |
| +VDD_MEM6 | AM27 | GND6 T6 |
| +VDD_MEM7 | AM29 | GND7 V10 |
| +VDD_MEM8 | AN16 | GND8 V34 |
| +VDD_MEM9 | BC29 | GND9 W5 |
| +VDD_MEM10 | AN20 | GND10 AA39 |
| +VDD_MEM11 | AN24 | GND11 AB22 |
| +VDD_MEM12 | AT17 | GND12 AB7 |
| +VDD_MEM13 | AP16 | GND13 AD22 |
| +VDD_MEM14 | AN22 | GND14 AE20 |
| +VDD_MEM15 | AP20 | GND15 AF24 |
| +VDD_MEM16 | AP24 | GND16 AG24 |
| +VDD_MEM17 | AV16 | GND17 AH35 |
| +VDD_MEM18 | AR16 | GND18 AK7 |
| +VDD_MEM19 | AR20 | GND19 AM28 |
| +VDD_MEM20 | AR24 | GND20 AT25 |
| +VDD_MEM21 | AW15 | GND21 AP30 |
| +VDD_MEM22 | AP22 | GND22 AR36 |
| +VDD_MEM23 | AP18 | GND23 AU10 |
| +VDD_MEM24 | AU16 | GND24 F28 |
| +VDD_MEM25 | AN18 | GND25 BC21 |
| +VDD_MEM26 | AU24 | GND26 AY9 |
| +VDD_MEM27 | AT21 | GND27 BC9 |
| +VDD_MEM28 | AY29 | GND28 D34 |
| +VDD_MEM29 | AV24 | GND29 F24 |
| +VDD_MEM30 | AU20 | GND30 G32 |
| +VDD_MEM31 | AU22 | GND31 H31 |
| +VDD_MEM32 | AW27 | GND32 K7 |
| +VDD_MEM33 | BC17 | GND33 M38 |
| +VDD_MEM34 | AV20 | GND34 M5 |
| +VDD_MEM35 | AY17 | GND35 M6 |
| +VDD_MEM36 | AY18 | GND36 M7 |
| +VDD_MEM37 | AM15 | GND37 M9 |
| +VDD_MEM38 | AU18 | GND38 N39 |
| +VDD_MEM39 | AY25 | GND39 N8 |
| +VDD_MEM40 | AY26 | GND40 P33 |
| +VDD_MEM41 | AW19 | GND41 P34 |
| +VDD_MEM42 | AW24 | GND42 P37 |
| +VDD_MEM43 | BC25 | GND43 P4 |
| +VDD_MEM44 | AL30 | GND44 P40 |
| +VDD_MEM45 | AM31 | GND45 P7 |
| | | GND46 R36 |
| | | GND47 R40 |
| | | GND48 R43 |
| | | GND49 R5 |
| | | GND50 T18 |
| | | GND51 T20 |
| | | GND52 AK11 |
| | | GND53 T24 |
| | | GND54 T26 |
| | | GND55 T33 |
| | | GND56 T34 |
| | | GND57 T35 |
| | | GND58 T37 |
| | | GND59 T38 |
| | | GND60 T7 |
| | | GND61 T9 |
| | | GND62 U18 |
| | | GND63 U20 |
| | | GND64 U22 |

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# MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


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|---|---|---|
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U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

| | | | | | | |
|---|---|---|---|---|---|---|
| =PEG_D2R_P<0> | F7 | PE0_RX0_P | PE0_TX0_P | C5 | =PEG_R2D_C_P<0> | |
| =PEG_D2R_N<0> | E7 | PE0_RX0_N | PE0_TX0_N | D4 | =PEG_R2D_C_N<0> | |
| =PEG_D2R_P<1> | D7 | PE0_RX1_P | PE0_TX1_P | C4 | =PEG_R2D_C_P<1> | |
| =PEG_D2R_N<1> | C7 | PE0_RX1_N | PE0_TX1_N | B4 | =PEG_R2D_C_N<1> | |
| =PEG_D2R_P<2> | E6 | PE0_RX2_P | PE0_TX2_P | A4 | =PEG_R2D_C_P<2> | |
| =PEG_D2R_N<2> | F6 | PE0_RX2_N | PE0_TX2_N | A3 | =PEG_R2D_C_N<2> | |
| =PEG_D2R_P<3> | E5 | PE0_RX3_P | PE0_TX3_P | B3 | =PEG_R2D_C_P<3> | |
| =PEG_D2R_N<3> | F5 | PE0_RX3_N | PE0_TX3_N | B2 | =PEG_R2D_C_N<3> | |
| =PEG_D2R_P<4> | E4 | PE0_RX4_P | PE0_TX4_P | C1 | =PEG_R2D_C_P<4> | |
| =PEG_D2R_N<4> | E3 | PE0_RX4_N | PE0_TX4_N | D1 | =PEG_R2D_C_N<4> | |
| =PEG_D2R_P<5> | C3 | PE0_RX5_P | PE0_TX5_P | D2 | =PEG_R2D_C_P<5> | |
| =PEG_D2R_N<5> | D3 | PE0_RX5_N | PE0_TX5_N | E1 | =PEG_R2D_C_N<5> | |
| =PEG_D2R_P<6> | G5 | PE0_RX6_P | PE0_TX6_P | E2 | =PEG_R2D_C_P<6> | |
| =PEG_D2R_N<6> | H5 | PE0_RX6_N | PE0_TX6_N | F2 | =PEG_R2D_C_N<6> | |
| =PEG_D2R_P<7> | J7 | PE0_RX7_P | PE0_TX7_P | F3 | =PEG_R2D_C_P<7> | |
| =PEG_D2R_N<7> | J6 | PE0_RX7_N | PE0_TX7_N | F4 | =PEG_R2D_C_N<7> | |
| =PEG_D2R_P<8> | J5 | PE0_RX8_P | PE0_TX8_P | G3 | =PEG_R2D_C_P<8> | |
| =PEG_D2R_N<8> | J4 | PE0_RX8_N | PE0_TX8_N | H4 | =PEG_R2D_C_N<8> | |
| =PEG_D2R_P<9> | L11 | PE0_RX9_P | PE0_TX9_P | H3 | =PEG_R2D_C_P<9> | |
| =PEG_D2R_N<9> | L10 | PE0_RX9_N | PE0_TX9_N | H2 | =PEG_R2D_C_N<9> | |
| =PEG_D2R_P<10> | L9 | PE0_RX10_P | PE0_TX10_P | H1 | =PEG_R2D_C_P<10> | |
| =PEG_D2R_N<10> | L8 | PE0_RX10_N | PE0_TX10_N | J1 | =PEG_R2D_C_N<10> | |
| =PEG_D2R_P<11> | L7 | PE0_RX11_P | PE0_TX11_P | J2 | =PEG_R2D_C_P<11> | |
| =PEG_D2R_N<11> | L6 | PE0_RX11_N | PE0_TX11_N | J3 | =PEG_R2D_C_N<11> | |
| =PEG_D2R_P<12> | N11 | PE0_RX12_P | PE0_TX12_P | K2 | =PEG_R2D_C_P<12> | |
| =PEG_D2R_N<12> | N10 | PE0_RX12_N | PE0_TX12_N | K3 | =PEG_R2D_C_N<12> | |
| =PEG_D2R_P<13> | N9 | PE0_RX13_P | PE0_TX13_P | L4 | =PEG_R2D_C_P<13> | |
| =PEG_D2R_N<13> | P9 | PE0_RX13_N | PE0_TX13_N | L3 | =PEG_R2D_C_N<13> | |
| =PEG_D2R_P<14> | N7 | PE0_RX14_P | PE0_TX14_P | M4 | =PEG_R2D_C_P<14> | |
| =PEG_D2R_N<14> | N6 | PE0_RX14_N | PE0_TX14_N | M3 | =PEG_R2D_C_N<14> | |
| =PEG_D2R_P<15> | N5 | PE0_RX15_P | PE0_TX15_P | M2 | =PEG_R2D_C_P<15> | |
| =PEG_D2R_N<15> | N4 | PE0_RX15_N | PE0_TX15_N | M1 | =PEG_R2D_C_N<15> | |

| | | | | | |
|---|---|---|---|---|---|
| | | PE0_REFCLK_P | E11 | PEG_CLK100M_P | 70 89 |
| | | PE0_REFCLK_N | D11 | PEG_CLK100M_N | 70 89 |
| PEG_PRSNT_L | C9 | PE0_PRSNT_16# Int PU | | | |
| MINI_CLKREQ_L | D5 | PE8_CLKREQ#/GPIO_49 Int PU | PE1_REFCLK_P | G11 | PCIE_CLK100M_MINI_P 31 89 |
| PCIE_MINI_PRSNT_L | D9 | PE8_PRSNT# Int PU | PE1_REFCLK_N | F11 | PCIE_CLK100M_MINI_N 31 89 |
| FW_CLKREQ_L | E8 | PEC_CLKREQ#/GPIO_50 Int PU | PE2_REFCLK_P | J11 | PCIE_CLK100M_FW_P 36 89 |
| PCIE_FW_PRSNT_L | C10 | PEC_PRSNT# Int PU | PE2_REFCLK_N | J10 | PCIE_CLK100M_FW_N 36 89 |
| EXCARD_CLKREQ_L | M15 | PED_CLKREQ#/GPIO_51 Int PU | PE3_REFCLK_P | G13 | PCIE_CLK100M_EXCARD_P 32 89 |
| PCIE_EXCARD_PRSNT_L | B10 | PED_PRSNT# Int PU | PE3_REFCLK_N | F13 | PCIE_CLK100M_EXCARD_N 32 89 |
| TP_PE4_CLKREQ_L | L16 | PEE_CLKREQ#/GPIO_16 Int PU | PE4_REFCLK_P | J13 | TP_PCIE_CLK100M_PE4P 9 |
| TP_PE4_PRSNT_L | L18 | PEE_PRSNT#/GPIO_46 Int PU | PE4_REFCLK_N | H13 | TP_PCIE_CLK100M_PE4N 9 |
| AUD_IP_PERIPHERAL_DET | M16 | PEF_CLKREQ#/GPIO_17 Int PU | PE5_REFCLK_P | L14 | TP_PCIE_CLK100M_PE5P |
| GMUX_JTAG_TCK_L | M18 | PEF_PRSNT#/GPIO_47 Int PU | PE5_REFCLK_N | K14 | TP_PCIE_CLK100M_PE5N |
| TP_MCP_GPIO_18 | M17 | PEG_CLKREQ#/GPIO_18 Int PU | PE6_REFCLK_P | N14 | TP_PCIE_CLK100M_PE6P |
| GMUX_JTAG_TDO | M19 | PEG_PRSNT#/GPIO_48 Int PU | PE6_REFCLK_N | M14 | TP_PCIE_CLK100M_PE6N |
| PCIE_WAKE_L | F17 | PE_WAKE# Int PU (S5) | PEX_RST0# | K11 | PCIE_RESET_L 9 26 |
| PCIE_MINI_D2R_P | K9 | PE1_RX0_P | PE1_TX0_P | D8 | PCIE_MINI_R2D_C_P 31 89 |
| PCIE_MINI_D2R_N | J9 | PE1_RX0_N | PE1_TX0_N | C8 | PCIE_MINI_R2D_C_N 31 89 |
| PCIE_FW_D2R_P | H9 | PE1_RX1_P | PE1_TX1_P | B8 | PCIE_FW_R2D_C_P 36 89 |
| PCIE_FW_D2R_N | G9 | PE1_RX1_N | PE1_TX1_N | A8 | PCIE_FW_R2D_C_N 36 89 |
| PCIE_EXCARD_D2R_P | F9 | PE1_RX2_P | PE1_TX2_P | A7 | PCIE_EXCARD_R2D_C_P 32 89 |
| PCIE_EXCARD_D2R_N | E9 | PE1_RX2_N | PE1_TX2_N | B7 | PCIE_EXCARD_R2D_C_N 32 89 |
| TP_PCIE_PE4_D2RP | H7 | PE1_RX3_P | PE1_TX3_P | B6 | TP_PCIE_PE4_R2D_CP 9 |
| TP_PCIE_PE4_D2RN | G7 | PE1_RX3_N | PE1_TX3_N | C6 | TP_PCIE_PE4_R2D_CN 9 |

=PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

| | |
|---|---|
| T17 | +DVDD0_PEX1 |
| W19 | +DVDD0_PEX2 |
| U17 | +DVDD0_PEX3 |
| V19 | +DVDD0_PEX4 |
| W16 | +DVDD0_PEX5 |
| W17 | +DVDD0_PEX6 |
| W18 | +DVDD0_PEX7 |
| U16 | +DVDD0_PEX8 |

=PP1V05_S0_MCP_PEX_DVDD1

| | |
|---|---|
| T19 | +DVDD1_PEX1 |
| U19 | +DVDD1_PEX2 |

PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

| | |
|---|---|
| T16 | +V_PLL_PEX |

MCP_PEX_CLK_COMP — A11 — PEX_CLK_COMP

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

=PP1V05_S0_MCP_PEX_AVDD0
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

| | |
|---|---|
| +AVDD0_PEX1 | Y12 |
| +AVDD0_PEX2 | AA12 |
| +AVDD0_PEX3 | AB12 |
| +AVDD0_PEX4 | M12 |
| +AVDD0_PEX5 | P12 |
| +AVDD0_PEX6 | R12 |
| +AVDD0_PEX7 | N12 |
| +AVDD0_PEX8 | T12 |
| +AVDD0_PEX9 | U12 |
| +AVDD0_PEX10 | AC12 |
| +AVDD0_PEX11 | AD12 |
| +AVDD0_PEX12 | V12 |
| +AVDD0_PEX13 | W12 |

=PP1V05_S0_MCP_PEX_AVDD1

| | |
|---|---|
| +AVDD1_PEX1 | M13 |
| +AVDD1_PEX2 | N13 |
| +AVDD1_PEX3 | P13 |

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

# MCP PCIe Interfaces

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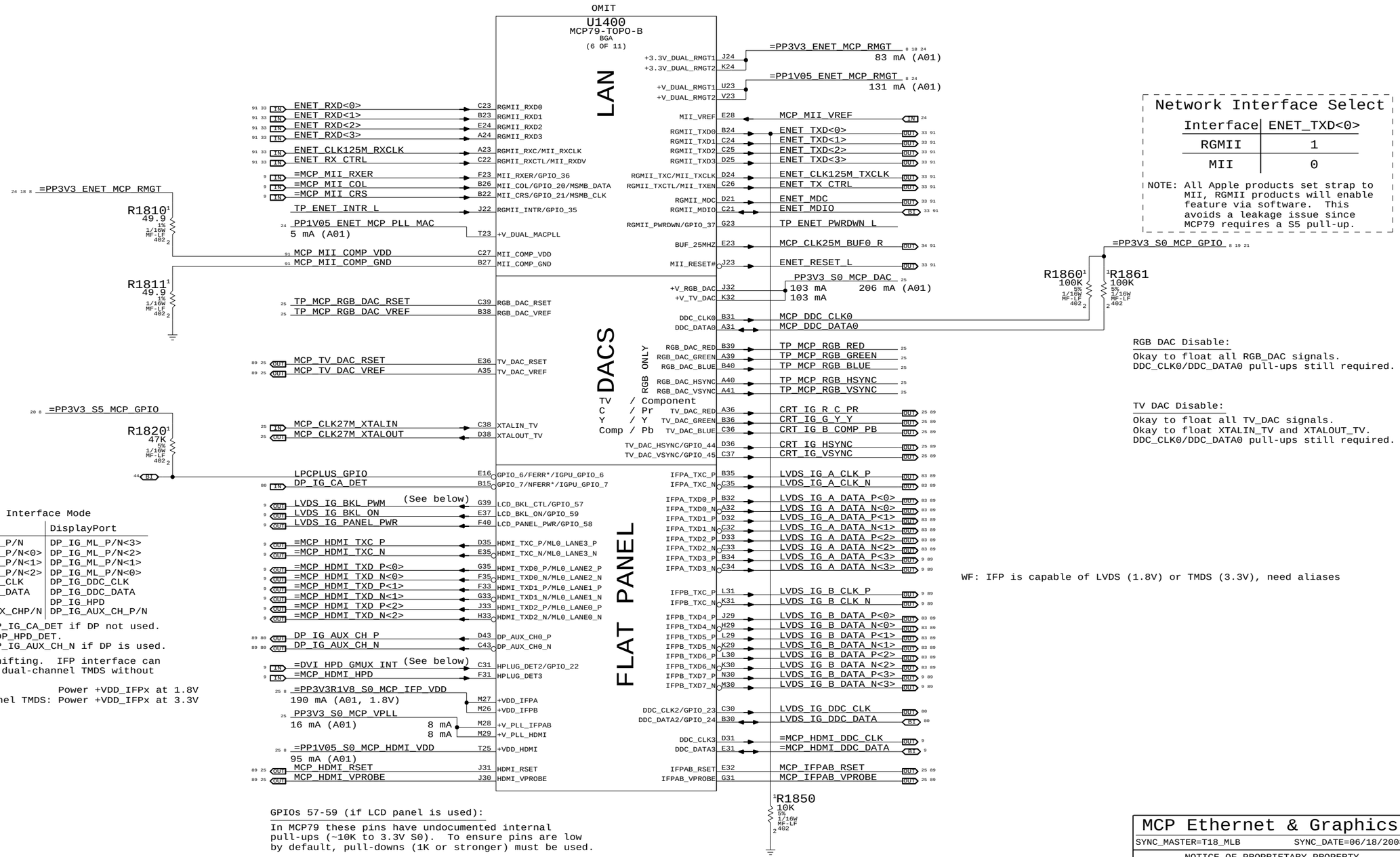


## Network Interface Select

| Interface | ENET_TXD<0> |
|---|---|
| RGMII | 1 |
| MII | 0 |

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

### RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

### TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

### Interface Mode

| MCP Signal | TMDS/HDMI | DisplayPort |
|---|---|---|
| =MCP_HDMI_TXC_P/N | TMDS_IG_TXC_P/N | DP_IG_ML_P/N<3> |
| =MCP_HDMI_TXD_P/N<0> | TMDS_IG_TXD_P/N<0> | DP_IG_ML_P/N<2> |
| =MCP_HDMI_TXD_P/N<1> | TMDS_IG_TXD_P/N<1> | DP_IG_ML_P/N<1> |
| =MCP_HDMI_TXD_P/N<2> | TMDS_IG_TXD_P/N<2> | DP_IG_ML_P/N<0> |
| =MCP_HDMI_DDC_CLK | TMDS_IG_DDC_CLK | DP_IG_DDC_CLK |
| =MCP_HDMI_DDC_DATA | TMDS_IG_DDC_DATA | DP_IG_DDC_DATA |
| =MCP_HDMI_HPD | TMDS_IG_HPD | DP_IG_HPD |
| DP_IG_AUX_CH_P/N | TP_DP_IG_AUX_CHP/N | DP_IG_AUX_CH_P/N |

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

### GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

### =DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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# MCP Ethernet & Graphics

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U1400
MCP79-TOPO-B
BGA
(7 OF 11)

## PCI

| | | | | | |
|---|---|---|---|---|---|
| 90 19 | PCI_REQ0_L | T2 | PCI_REQ0# | | |
| 90 19 | PCI_REQ1_L | V9 | PCI_REQ1#/FANRPM2 | | |
| 19 OUT | CRTMUX_SEL_TV_L | T3 | PCI_REQ2#/GPIO_40/RS232_DSR# | PCI_GNT2#/GPIO_41/RS232_DTR# | R4 GMUX_JTAG_TMS OUT 9 |
| 59 9 OUT | AUD_IPHS_SWITCH_EN | U9 | PCI_REQ3#/GPIO_38/RS232_CTS# | PCI_GNT3#/GPIO_39/RS232_RTS# | U11 GMUX_JTAG_TDI OUT 9 |
| 19 IN | MCP_RS232_SIN_L | T4 | PCI_REQ4#/GPIO_52/RS232_SIN# | PCI_GNT4#/GPIO_53/RS232_SOUT# | P3 MCP_RS232_SOUT_L OUT 19 |
| 90 13 BI | MCP_DEBUG<0> | AC3 | PCI_AD0 | PCI_CBE0# | AA3 TP_PCI_C_BE_L<0> |
| 90 13 BI | MCP_DEBUG<1> | AE10 | PCI_AD1 | PCI_CBE1# | AA6 TP_PCI_C_BE_L<1> |
| 90 13 BI | MCP_DEBUG<2> | AC4 | PCI_AD2 | PCI_CBE2# | AA11 TP_PCI_C_BE_L<2> |
| 90 13 BI | MCP_DEBUG<3> | AE11 | PCI_AD3 | PCI_CBE3# | W10 TP_PCI_C_BE_L<3> |
| 90 13 BI | MCP_DEBUG<4> | AB3 | PCI_AD4 | | |
| 90 13 BI | MCP_DEBUG<5> | AC6 | PCI_AD5 | PCI_DEVSEL# | AA9 TP_PCI_DEVSEL_L |
| 90 13 BI | MCP_DEBUG<6> | AB2 | PCI_AD6 | PCI_FRAME# | Y4 TP_PCI_FRAME_L |
| 90 13 BI | MCP_DEBUG<7> | AC7 | PCI_AD7 | PCI_IRDY# | AA10 TP_PCI_IRDY_L |
| | TP_PCI_AD<8> | AC8 | PCI_AD8 | PCI_PAR | Y1 TP_PCI_PAR |
| | TP_PCI_AD<9> | AA2 | PCI_AD9 | PCI_PERR#/GPIO_43/RS232_DCD# | AB9 TP_PCI_PERR_L |
| | TP_PCI_AD<10> | AC9 | PCI_AD10 | PCI_SERR# | AA7 TP_PCI_SERR_L |
| | TP_PCI_AD<11> | AC10 | PCI_AD11 | PCI_STOP# | Y2 TP_PCI_STOP_L |
| | TP_PCI_AD<12> | AC11 | PCI_AD12 | PCI_PME#/GPIO_30 Int PU (S5) | T1 PM_LATRIGGER_L OUT 13 23 |
| | TP_PCI_AD<13> | AA1 | PCI_AD13 | | |
| | TP_PCI_AD<14> | AA5 | PCI_AD14 | PCI_RESET0# | R10 MEM_VTT_EN_R OUT 26 |
| | TP_PCI_AD<15> | Y5 | PCI_AD15 | PCI_RESET1# | R11 TP_PCI_RESET1_L |
| | TP_PCI_AD<16> | W3 | PCI_AD16 | | |
| | TP_PCI_AD<17> | W6 | PCI_AD17 | | |
| | TP_PCI_AD<18> | W4 | PCI_AD18 | | |
| | TP_PCI_AD<19> | W7 | PCI_AD19 | | |
| | TP_PCI_AD<20> | V3 | PCI_AD20 | PCI_CLK0 | R6 TP_PCI_CLK0 |
| | TP_PCI_AD<21> | W8 | PCI_AD21 | PCI_CLK1 | R7 TP_PCI_CLK1 |
| | TP_PCI_AD<22> | V2 | PCI_AD22 | PCI_CLK2 | R8 90 PCI_CLK33M_MCP_R |
| | TP_PCI_AD<23> | W9 | PCI_AD23 | | |
| | TP_PCI_AD<24> | U3 | PCI_AD24 | | |
| | TP_PCI_AD<25> | W11 | PCI_AD25 | | |
| | TP_PCI_AD<26> | U2 | PCI_AD26 | | |
| | TP_PCI_AD<27> | U5 | PCI_AD27 | | |
| | TP_PCI_AD<28> | U1 | PCI_AD28 | | |
| | TP_PCI_AD<29> | U6 | PCI_AD29 | PCI_CLKIN | R9 90 PCI_CLK33M_MCP |
| | TP_PCI_AD<30> | T5 | PCI_AD30 | | |
| | TP_PCI_AD<31> | U7 | PCI_AD31 | | |
| | TP_PCI_INTW_L | P2 | PCI_INTW# | | |
| | TP_PCI_INTX_L | N3 | PCI_INTX# | | |
| | TP_PCI_INTY_L | N2 | PCI_INTY# | | |
| | TP_PCI_INTZ_L | N1 | PCI_INTZ# | | |
| | TP_PCI_TRDY_L | Y3 | PCI_TRDY# | | |
| 44 42 IN | PM_CLKRUN_L | AD11 | PCI_CLKRUN#/GPIO_42 | | |
| 36 IN | FW_PME_L | AE2 | LPC_DRQ1#/GPIO_19 Int PU | | |
| | TP_LPC_DRQ0_L | AE1 | LPC_DRQ0# Int PU | | |
| 44 42 BI | LPC_SERIRQ | AE6 | LPC_SERIRQ Int PU | | |

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

## LPC

| | | | | | |
|---|---|---|---|---|---|
| PCI_FRAME# | AD4 | 4 | LPC_FRAME_R_L | R1960 22 | LPC_FRAME_L OUT 42 44 83 90 |
| LPC_PWRDWN#/GPIO_54/EXT_NMI# | AE12 | | LPC_PWRDWN_L | | OUT 42 44 |
| LPC_RESET0# | AE5 | | LPC_RESET_L | | OUT 26 83 90 |
| LPC_AD0 | AD3 | | LPC_AD_R<0> | R1950 22 | LPC_AD<0> BI 42 44 83 90 |
| LPC_AD1 | AD2 | | LPC_AD_R<1> | R1951 22 | LPC_AD<1> BI 42 44 83 90 |
| LPC_AD2 | AD1 | | LPC_AD_R<2> | R1952 22 | LPC_AD<2> BI 42 44 83 90 |
| LPC_AD3 | AD5 | | LPC_AD_R<3> | R1953 22 | LPC_AD<3> BI 42 44 83 90 |
| LPC_CLK0 | AE9 | | LPC_CLK33M_SMC_R | | OUT 26 90 |

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

## GND

| | | | |
|---|---|---|---|
| U24 | GND65 | GND98 | Y26 |
| U26 | GND66 | GND99 | Y27 |
| U39 | GND67 | GND100 | AB18 |
| U4 | GND68 | GND101 | H34 |
| U8 | GND69 | GND102 | AB20 |
| V16 | GND70 | GND103 | AB21 |
| V17 | GND71 | GND104 | AB23 |
| V18 | GND72 | GND105 | AB24 |
| V20 | GND73 | GND106 | AB25 |
| V22 | GND74 | GND107 | AB26 |
| V24 | GND75 | GND108 | AB27 |
| V26 | GND76 | GND109 | AB28 |
| V27 | GND77 | GND110 | AB34 |
| V28 | GND78 | GND111 | AB37 |
| V33 | GND79 | GND112 | AB4 |
| V37 | GND80 | GND113 | AB40 |
| V4 | GND81 | GND114 | AC22 |
| V40 | GND82 | GND115 | AC36 |
| V7 | GND83 | GND116 | AC40 |
| W20 | GND84 | GND117 | AB33 |
| W22 | GND85 | GND118 | AC5 |
| W24 | GND86 | GND119 | AD16 |
| W36 | GND87 | GND120 | AD17 |
| W40 | GND88 | GND121 | AD18 |
| W43 | GND89 | GND122 | AD19 |
| Y16 | GND90 | GND123 | AD20 |
| Y17 | GND91 | GND124 | AD24 |
| Y18 | GND92 | GND125 | AD25 |
| Y19 | GND93 | GND126 | AD26 |
| Y20 | GND94 | GND127 | AD27 |
| Y22 | GND95 | GND128 | AD28 |
| Y24 | GND96 | GND129 | AD33 |
| Y25 | GND97 | GND130 | AD34 |

21 18 8 =PP3V3_S0_MCP_GPIO

| | | | |
|---|---|---|---|
| 19 | MCP_RS232_SOUT_L | R1989 | 8.2K 5% 1/16W MF-LF 402 |
| 90 19 | PCI_REQ0_L | R1990 | 8.2K 5% 1/16W MF-LF 402 |
| 90 19 | PCI_REQ1_L | R1991 | 8.2K 5% 1/16W MF-LF 402 |
| 19 | CRTMUX_SEL_TV_L | R1992 | 8.2K 5% 1/16W MF-LF 402 |
| 19 | MCP_RS232_SIN_L | R1994 | 8.2K 5% 1/16W MF-LF 402 |

# MCP PCI & LPC

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## U1400
MCP79-TOPO-B
BGA
(8 OF 11)

### SATA

| | | | |
|---|---|---|---|
| SATA_HDD_R2D_C_P | AJ7 | SATA_A0_TX_P | 89 39 OUT |
| SATA_HDD_R2D_C_N | AJ6 | SATA_A0_TX_N | 89 39 OUT |
| SATA_HDD_D2R_N | AJ5 | SATA_A0_RX_N | 89 39 IN |
| SATA_HDD_D2R_P | AJ4 | SATA_A0_RX_P | 89 39 IN |
| SATA_ODD_R2D_C_P | AJ11 | SATA_A1_TX_P | 89 39 OUT |
| SATA_ODD_R2D_C_N | AJ10 | SATA_A1_TX_N | 89 39 OUT |
| SATA_ODD_D2R_N | AJ9 | SATA_A1_RX_N | 89 39 IN |
| SATA_ODD_D2R_P | AK9 | SATA_A1_RX_P | 89 39 IN |
| TP_SATA_C_R2D_CP | AK2 | SATA_B0_TX_P | |
| TP_SATA_C_R2D_CN | AJ3 | SATA_B0_TX_N | |
| TP_SATA_C_D2RN | AJ2 | SATA_B0_RX_N | |
| TP_SATA_C_D2RP | AJ1 | SATA_B0_RX_P | |
| TP_SATA_D_R2D_CP | AM4 | SATA_B1_TX_P | |
| TP_SATA_D_R2D_CN | AL3 | SATA_B1_TX_N | |
| TP_SATA_D_D2RN | AL4 | SATA_B1_RX_N | |
| TP_SATA_D_D2RP | AK3 | SATA_B1_RX_P | |
| TP_SATA_E_R2D_CP | AN1 | SATA_C0_TX_P | |
| TP_SATA_E_R2D_CN | AM1 | SATA_C0_TX_N | |
| TP_SATA_E_D2RN | AM2 | SATA_C0_RX_N | |
| TP_SATA_E_D2RP | AM3 | SATA_C0_RX_P | |
| TP_SATA_F_R2D_CP | AP3 | SATA_C1_TX_P | |
| TP_SATA_F_R2D_CN | AP2 | SATA_C1_TX_N | |
| TP_SATA_F_D2RN | AN3 | SATA_C1_RX_N | |
| TP_SATA_F_D2RP | AN2 | SATA_C1_RX_P | |
| TP_MCP_SATALED_L | E12 | SATA_LED# | |

24 PP1V05_S0_MCP_PLL_SATA — AE16 +V_PLL_SATA
84 mA (A01)

8 =PP1V05_S0_MCP_SATA_DVDD0 — 43 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

| | | |
|---|---|---|
| AF19 | +DVDD0_SATA1 | |
| AG16 | +DVDD0_SATA2 | |
| AG17 | +DVDD0_SATA3 | |
| AG19 | +DVDD0_SATA4 | |

9 =PP1V05_S0_MCP_SATA_DVDD1

| | | |
|---|---|---|
| AH17 | +DVDD1_SATA1 | |
| AH19 | +DVDD1_SATA2 | |

8 =PP1V05_S0_MCP_SATA_AVDD0 — 127 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

| | | |
|---|---|---|
| AJ12 | +AVDD0_SATA1 | |
| AN11 | +AVDD0_SATA2 | |
| AK12 | +AVDD0_SATA3 | |
| AK13 | +AVDD0_SATA4 | |
| AL12 | +AVDD0_SATA5 | |
| AM11 | +AVDD0_SATA6 | |
| AM12 | +AVDD0_SATA7 | |
| AN12 | +AVDD0_SATA8 | |
| AL13 | +AVDD0_SATA9 | |

9 =PP1V05_S0_MCP_SATA_AVDD1

| | | |
|---|---|---|
| AN14 | +AVDD1_SATA1 | |
| AL14 | +AVDD1_SATA2 | |
| AM13 | +AVDD1_SATA3 | |
| AM14 | +AVDD1_SATA4 | |

89 MCP_SATA_TERMP — AE3 SATA_TERMP

R2010 2.49K 1% 1/16W MF-LF 402

### USB

External A
| | | | |
|---|---|---|---|
| USB0_P | C29 | USB_EXTA_P | BI 40 90 |
| USB0_N | D29 | USB_EXTA_N | BI 40 90 |

AirPort (PCIe Mini-Card)
| | | | |
|---|---|---|---|
| USB1_P | C28 | USB_MINI_P | BI 9 90 |
| USB1_N | D28 | USB_MINI_N | BI 9 90 |

External D
| | | | |
|---|---|---|---|
| USB2_P | A28 | USB_EXTD_P | BI 9 90 |
| USB2_N | B28 | USB_EXTD_N | BI 9 90 |

Camera
| | | | |
|---|---|---|---|
| USB3_P | F29 | USB_CAMERA_P | BI 31 90 |
| USB3_N | G29 | USB_CAMERA_N | BI 31 90 |

IR
| | | | |
|---|---|---|---|
| USB4_P | K27 | USB_IR_P | BI 41 90 |
| USB4_N | L27 | USB_IR_N | BI 41 90 |

Geyser Trackpad/Keyboard
| | | | |
|---|---|---|---|
| USB5_P | J26 | USB_TPAD_P | BI 50 90 |
| USB5_N | J27 | USB_TPAD_N | BI 50 90 |

Bluetooth
| | | | |
|---|---|---|---|
| USB6_P | F27 | USB_BT_P | BI 31 90 |
| USB6_N | G27 | USB_BT_N | BI 31 90 |

External B
| | | | |
|---|---|---|---|
| USB7_P | D27 | USB_EXTB_P | BI 40 90 |
| USB7_N | E27 | USB_EXTB_N | BI 40 90 |

ExpressCard
| | | | |
|---|---|---|---|
| USB8_P | K25 | USB_EXCARD_P | BI 32 90 |
| USB8_N | L25 | USB_EXCARD_N | BI 32 90 |

External C
| | | | |
|---|---|---|---|
| USB9_P | H25 | USB_EXTC_P | BI 9 90 |
| USB9_N | J25 | USB_EXTC_N | BI 9 90 |

| | | |
|---|---|---|
| USB10_P | F25 | TP_USB_10P |
| USB10_N | G25 | TP_USB_10N |
| USB11_P | K23 | TP_USB_11P |
| USB11_N | L23 | TP_USB_11N |

| | | | |
|---|---|---|---|
| USB_OC0#/GPIO_25 | L21 | USB_EXTA_OC_L | IN 40 |
| USB_OC1#/GPIO_26 | K21 | USB_EXTB_OC_L | IN 40 |
| USB_OC2#/GPIO_27/MGPIO | J21 | USB_EXTC_OC_L | IN |
| USB_OC3#/GPIO_28/MGPIO | H21 | EXCARD_OC_L | IN 32 43 |

=PP3V3_S5_MCP_GPIO 8 18

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

+V_PLL_USB — L28 — PP3V3_S0_MCP_PLL_USB 24
19 mA (A01)

USB_RBIAS_GND — A27 — 90 MCP_USB_RBIAS_GND

R2060 806 1% 1/10W MF-LF 402

| | | |
|---|---|---|
| GND131 | AD35 | |
| GND132 | AD37 | |
| GND133 | AD38 | |
| GND134 | AE22 | |
| GND135 | AE24 | |
| GND136 | AE39 | |
| GND137 | AE4 | |
| GND138 | AD6 | |
| GND139 | AF16 | |
| GND140 | AF17 | |
| GND141 | AF18 | |
| GND142 | AF20 | |
| GND143 | AF22 | |
| GND144 | AF26 | |
| GND145 | AF27 | |
| GND146 | AF28 | |
| GND147 | AF33 | |
| GND148 | AF34 | |
| GND149 | AF37 | |
| GND150 | AF40 | |
| GND151 | AG18 | |
| GND152 | AG20 | |
| GND153 | AG22 | |
| GND154 | AG26 | |
| GND155 | AG36 | |
| GND156 | AG40 | |
| GND157 | AH18 | |
| GND158 | AH20 | |
| GND159 | AH22 | |
| GND160 | AH24 | |

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

# MCP SATA & USB

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U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

HDA_SDIN0 → G15 HDA_SDATA_IN0 (Int PD)
TP_MLB_RAM_SIZE → J14 HDA_SDATA_IN1/GPIO_2/PS2_KB_CLK (Int PD)
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) → J15 HDA_SDATA_IN2/GPIO_3/PS2_KB_DATA (Int PD)
=PP3V3R1V5_S0_MCP_HDA → R2110 49.9 1% 1/16W MF-LF 402 → MCP_HDA_PULLDN_COMP → A15 HDA_PULLDN_COMP
PP1V05_S0_MCP_PLL_NV 37 mA (A01) 20 mA 17 mA → AE18 +V_PLL_NV_H, AE17 +V_PLL_SP_SPREF

=PP3V3R1V5_S0_MCP_HDA 7 mA (A01)
+V_DUAL_HDA1 J16, +V_DUAL_HDA2 K16 → R2160 8.2K 5% 1/16W MF-LF 402

HDA_SDATA_OUT F15 → HDA_SDOUT_R → R2170 22 → HDA_SDOUT
HDA_BITCLK E15 → HDA_BIT_CLK_R → R2171 22 → HDA_BIT_CLK
HDA_RESET# K15 → HDA_RST_R_L → R2172 22 → HDA_RST_L
HDA_SYNC L15 → HDA_SYNC_R → R2173 22 → HDA_SYNC

MISC

PP3V3_G3_RTC → R2120 49.9K, R2121 49.9K
=SPI_CS1_R_L_USE_MLB → L24 GPIO_1/PWRDN_OK/SPI_CS1
SMC_ADAPTER_EN → L26 GPIO_12/SUS_STAT#/ACCLMTR
TP_SB_A20GATE → K13 A20GATE Int PU
TP_MCP_KBDRSTIN_L → L13 KBRDRSTIN# Int PU
SMC_WAKE_SCI_L → C19 SIO_PME# Int PU (S5)
SMC_RUNTIME_SCI_L → C18 EXT_SMI/GPIO_32# Int PU (S5)
SM_INTRUDER_L → B20 INTRUDER#
TP_MCP_LID_L → M25 LID# Int PU (S5)
PM_BATLOW_L → M24 LLB# Int PU (S5)
PM_DPRSLPVR → M22 CPU_DPRSLPVR
PM_PWRBTN_L → C16 PWRBTN# Int PU (S5)
PM_SYSRST_DEBOUNCE_L → D16 RSTBTN# Int PU
RTC_RST_L → C20 RTC_RST#
PM_RSMRST_L → D20 PWRGD_SB
MCP_PS_PWRGD → E20 PS_PWRGD
MCP_CPU_VLD → C17 CPU_VLD
JTAG_MCP_TDI → E19 JTAG_TDI Int PU
JTAG_MCP_TDO ← F19 JTAG_TDO
JTAG_MCP_TMS → J19 JTAG_TMS Int PU
JTAG_MCP_TRST_L → J18 JTAG_TRST#
JTAG_MCP_TCK → G19 JTAG_TCK
MCP_CLK25M_XTALIN → A16 XTALIN
MCP_CLK25M_XTALOUT ← B16 XTALOUT
RTC_CLK32K_XTALIN → A19 XTALIN_RTC
RTC_CLK32K_XTALOUT ← B19 XTALOUT_RTC
R2150 10K, R2151 100K

SMB_CLK0 L19, SMB_DATA0 K19 → SMBUS_MCP_0_CLK, SMBUS_MCP_0_DATA
SMB_CLK1/MSMB_CLK G21, SMB_DATA1/MSMB_DATA F21 → SMBUS_MCP_1_CLK, SMBUS_MCP_1_DATA
SMB_ALERT#/GPIO_64 M23 → AP_PWR_EN
(MGPIO2) FANRPM0/GPIO_60 B12 → MEM_EVENT_L
FANCTL0/GPIO_61 A12 → ODD_PWR_EN_L
(MGPIO3) FANRPM1/GPIO_63 D12 → SMC_IG_THROTTLE_L
FANCTL1/GPIO_62 C12 → ARB_DETECT
CPUVDD_EN D17 → MCP_CPUVDD_EN
SPI_CS0/GPIO_10 C14 → SPI_CS0_R_L
SPI_CLK/GPIO_11 D13 → SPI_CLK_R
SPI_DI/GPIO_8 C15 ← SPI_MISO
SPI_DO/GPIO_9 B14 → SPI_MOSI_R
SUS_CLK/GPIO_34 B18 → PM_CLK32K_SUSCLK_R
BUF_SIO_CLK AE7 → TP_MCP_BUF_SIO_CLK
TEST_MODE_EN K22 → MCP_TEST_MODE_EN
PKG_TEST L22
R2163 10K, R2190 1K

THERM_DIODE_P B11, THERM_DIODE_N C11 → MCP_THMDIODE_P, MCP_THMDIODE_N
MCP_VID0/GPIO_13 L20, MCP_VID1/GPIO_14 M20, MCP_VID2/GPIO_15 M21 → MCP_VID<0>, MCP_VID<1>, MCP_VID<2>
SPKR C13 → MCP_SPKR
SLP_S3# G17 → PM_SLP_S3_L
SLP_RMGT# J17 → PM_SLP_RMGT_L
SLP_S5# H17 → PM_SLP_S4_L
HDA_DOCK_EN#/GPIO_4/PS2_MS_CLK K17 → MCP_GPIO_4
HDA_DOCK_RST#/GPIO_5/PS2_MS_DATA L17 → AUD_I2C_INT_L

=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K
BOOT_MODE_USER
R2181 10K
USER mode: Normal
SAFE mode: For ROMSIP recovery
Connects to SMC for automatic recovery.

## BIOS Boot Select

| I/F | HDA_SDOUT | LPC_FRAME# |
|---|---|---|
| LPC | 0 | 0 |
| PCI | 0 | 1 |
| SPI0 | 1 | 0 |
| SPI1 | 1 | 1 |

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

## BUF_SIO_CLK Frequency

| Frequency | HDA_SYNC |
|---|---|
| 24 MHz | 1 |
| 14.31818 MHz | 0 |

## SPI Frequency Select

| Frequency | SPI_DO | SPI_CLK |
|---|---|---|
| 31 MHz | 0 | 0 |
| 42 MHz | 0 | 1 |
| 25 MHz | 1 | 0 |
| 1 MHz | 1 | 1 |

NOTE: Straps not provided on this page.

## HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R, HDA_BIT_CLK_R, HDA_RST_R_L, HDA_SYNC_R
C2170 10PF, C2172 10PF, C2171 10PF, C2173 10PF (5% 50V CERM 402)

=PP3V3_S0_MCP_GPIO
R2140 10K, R2141 10K, R2142 10K, R2143 10K
MCP_GPIO_4, AUD_I2C_INT_L, MEM_EVENT_L, SMC_IG_THROTTLE_L
ARB_DETECT
R2147 100K

=PP3V3_S3_MCP_GPIO
R2154 100K
AP_PWR_EN

MCP_VID<0>, MCP_VID<1>, MCP_VID<2>
R2155 22K, R2156 22K, R2157 22K

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

## MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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|---|---|---|
| D | 051-7902 | D |

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OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

| | | | |
|---|---|---|---|
| AH26 | GND161 | GND253 | AV40 |
| AH33 | GND162 | GND254 | BA1 |
| AH34 | GND163 | GND255 | BA4 |
| AH37 | GND164 | GND256 | AW31 |
| AH38 | GND165 | GND257 | AY6 |
| AJ39 | GND166 | GND258 | L35 |
| AJ8 | GND167 | GND259 | BC33 |
| AK10 | GND168 | GND260 | BC37 |
| AK33 | GND169 | GND261 | BC41 |
| AK34 | GND170 | GND262 | AY14 |
| AK37 | GND171 | GND263 | BC5 |
| AK4 | GND172 | GND264 | C2 |
| AK40 | GND173 | GND265 | D10 |
| AL36 | GND174 | GND266 | D14 |
| AL40 | GND175 | GND267 | D15 |
| AL5 | GND176 | GND268 | D18 |
| AM10 | GND177 | GND269 | D19 |
| AM16 | GND178 | GND270 | D22 |
| AM18 | GND179 | GND271 | D23 |
| AM20 | GND180 | GND272 | D26 |
| AM22 | GND181 | GND273 | D30 |
| AM24 | GND182 | GND274 | D37 |
| AM26 | GND183 | GND275 | D6 |
| AM30 | GND184 | GND276 | E13 |
| AM34 | GND185 | GND277 | E17 |
| AM35 | GND186 | GND278 | E21 |
| AM37 | GND187 | GND279 | E25 |
| AM38 | GND188 | GND280 | E29 |
| AM5 | GND189 | GND281 | E33 |
| AM6 | GND190 | GND282 | F12 |
| AM7 | GND191 | GND283 | F16 |
| AM9 | GND192 | GND284 | F32 |
| AP26 | GND193 | GND285 | F8 |
| AN28 | GND194 | GND286 | G10 |
| AN30 | GND195 | GND287 | G12 |
| AN39 | GND196 | GND288 | G14 |
| AN4 | GND197 | GND289 | G16 |
| Y7 | GND198 | GND290 | BC12 |
| AP10 | GND199 | GND291 | G22 |
| AU26 | GND200 | GND292 | G24 |
| AP14 | GND201 | GND293 | AW20 |
| AU14 | GND202 | GND294 | G34 |
| AP28 | GND203 | GND295 | G4 |
| AP32 | GND204 | GND296 | G43 |
| AP34 | GND205 | GND297 | G6 |
| AP36 | GND206 | GND298 | G8 |
| AP37 | GND207 | GND299 | H11 |
| AP4 | GND208 | GND300 | H15 |
| AP40 | GND209 | GND301 | AW35 |
| AP7 | GND210 | GND302 | H23 |
| AW23 | GND211 | GND303 | AN8 |
| AR28 | GND212 | GND304 | G40 |
| AR32 | GND213 | GND305 | J12 |
| AR40 | GND214 | GND306 | J8 |
| AT10 | GND215 | GND307 | K10 |
| AR12 | GND216 | GND308 | K12 |
| AT13 | GND217 | GND309 | K18 |
| AT29 | GND218 | GND310 | K26 |
| AT33 | GND219 | GND311 | K37 |
| AT6 | GND220 | GND312 | K4 |
| AT7 | GND221 | GND313 | K40 |
| AT9 | GND222 | GND314 | K8 |
| AY21 | GND223 | GND315 | AU1 |
| AY22 | GND224 | GND316 | L40 |
| L12 | GND225 | GND317 | L43 |
| AU12 | GND226 | GND318 | L5 |
| AU28 | GND227 | GND319 | M10 |
| AP33 | GND228 | GND320 | M34 |
| AU32 | GND229 | GND321 | M35 |
| AR30 | GND230 | GND322 | M37 |
| AU36 | GND231 | GND323 | Y28 |
| AU38 | GND232 | GND324 | Y33 |
| AU4 | GND233 | GND325 | Y34 |
| G28 | GND234 | GND326 | Y35 |
| F20 | GND235 | GND327 | Y37 |
| AV28 | GND236 | GND328 | Y38 |
| AV32 | GND237 | GND329 | AB17 |
| AV36 | GND238 | GND330 | AB16 |
| AV4 | GND239 | GND331 | AN26 |
| AV7 | GND240 | GND332 | AD7 |
| AW11 | GND241 | GND333 | M11 |
| G20 | GND242 | GND334 | AA4 |
| AR43 | GND243 | GND335 | AB19 |
| AW43 | GND244 | GND336 | AY13 |
| AY10 | GND245 | GND337 | P11 |
| AV12 | GND246 | GND338 | Y6 |
| AY30 | GND247 | GND339 | T11 |
| AY33 | GND248 | GND340 | V11 |
| AY34 | GND249 | GND341 | Y11 |
| AY37 | GND250 | GND342 | AH16 |
| AY38 | GND251 | GND343 | T22 |
| AY41 | GND252 | | |

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

46 24 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

| | | | | | |
|---|---|---|---|---|---|
| AA25 | +VDD_CORE1 | +VTT_CPU1 | R32 | =PP1V05_S0_MCP_FSB 8 9 14 24 | |
| AC23 | +VDD_CORE2 | +VTT_CPU2 | AC32 | 1139 mA | 1182 mA (A01) |
| U25 | +VDD_CORE3 | +VTT_CPU3 | E40 | | |
| AH12 | +VDD_CORE4 | +VTT_CPU4 | J36 | | |
| AG10 | +VDD_CORE5 | +VTT_CPU5 | N32 | | |
| AG5 | +VDD_CORE6 | +VTT_CPU6 | T32 | | |
| Y21 | +VDD_CORE7 | +VTT_CPU7 | U32 | | |
| Y23 | +VDD_CORE8 | +VTT_CPU8 | V32 | | |
| AA16 | +VDD_CORE9 | +VTT_CPU9 | W32 | | |
| AA26 | +VDD_CORE10 | +VTT_CPU10 | P31 | | |
| AA27 | +VDD_CORE11 | +VTT_CPU11 | AF32 | | |
| AA28 | +VDD_CORE12 | +VTT_CPU12 | AE32 | | |
| AC16 | +VDD_CORE13 | +VTT_CPU13 | AH32 | | |
| AC17 | +VDD_CORE14 | +VTT_CPU14 | AJ32 | | |
| AC18 | +VDD_CORE15 | +VTT_CPU15 | AK31 | | |
| AC19 | +VDD_CORE16 | +VTT_CPU16 | AK32 | | |
| AC20 | +VDD_CORE17 | +VTT_CPU17 | AD32 | | |
| AC21 | +VDD_CORE18 | +VTT_CPU18 | AL31 | | |
| AA17 | +VDD_CORE19 | +VTT_CPU19 | AB32 | | |
| AC24 | +VDD_CORE20 | +VTT_CPU20 | B41 | | |
| AC25 | +VDD_CORE21 | +VTT_CPU21 | B42 | | |
| AC26 | +VDD_CORE22 | +VTT_CPU22 | C40 | | |
| AC27 | +VDD_CORE23 | +VTT_CPU23 | C41 | | |
| AC28 | +VDD_CORE24 | +VTT_CPU24 | C42 | | |
| AD21 | +VDD_CORE25 | +VTT_CPU25 | D39 | | |
| AD23 | +VDD_CORE26 | +VTT_CPU26 | D40 | | |
| W27 | +VDD_CORE27 | +VTT_CPU27 | D41 | | |
| V25 | +VDD_CORE28 | +VTT_CPU28 | E38 | | |
| AA18 | +VDD_CORE29 | +VTT_CPU29 | E39 | | |
| AE19 | +VDD_CORE30 | +VTT_CPU30 | F37 | | |
| AE21 | +VDD_CORE31 | +VTT_CPU31 | F38 | | |
| AE23 | +VDD_CORE32 | +VTT_CPU32 | F39 | | |
| AE25 | +VDD_CORE33 | +VTT_CPU33 | G36 | | |
| AE26 | +VDD_CORE34 | +VTT_CPU34 | G37 | | |
| AE27 | +VDD_CORE35 | +VTT_CPU35 | G38 | | |
| AE28 | +VDD_CORE36 | +VTT_CPU36 | H35 | | |
| AF10 | +VDD_CORE37 | +VTT_CPU37 | H37 | | |
| AF11 | +VDD_CORE38 | +VTT_CPU38 | J34 | | |
| AA19 | +VDD_CORE39 | +VTT_CPU39 | J35 | | |
| AF2 | +VDD_CORE40 | +VTT_CPU40 | K33 | | |
| AF21 | +VDD_CORE41 | +VTT_CPU41 | K34 | | |
| AF23 | +VDD_CORE42 | +VTT_CPU42 | K35 | | |
| AF25 | +VDD_CORE43 | +VTT_CPU43 | L32 | | |
| AF3 | +VDD_CORE44 | +VTT_CPU44 | L33 | | |
| AF4 | +VDD_CORE45 | +VTT_CPU45 | L34 | | |
| AF7 | +VDD_CORE46 | +VTT_CPU46 | M31 | | |
| AH23 | +VDD_CORE47 | +VTT_CPU47 | M32 | | |
| AF9 | +VDD_CORE48 | +VTT_CPU48 | M33 | | |
| AA20 | +VDD_CORE49 | +VTT_CPU49 | N31 | | |
| AG11 | +VDD_CORE50 | +VTT_CPU50 | P32 | | |
| AG12 | +VDD_CORE51 | +VTT_CPU51 | Y32 | | |
| AG21 | +VDD_CORE52 | +VTT_CPU52 | AA32 | | |
| AG23 | +VDD_CORE53 | | | | |
| AG25 | +VDD_CORE54 | +VTT_CPUCLK | AG32 | 43 mA | |
| AG3 | +VDD_CORE55 | | | | |
| AG4 | +VDD_CORE56 | | | | |
| AA21 | +VDD_CORE57 | | | | |
| AG6 | +VDD_CORE58 | | | | |
| AG7 | +VDD_CORE59 | | | =PP3V3_S0_MCP 8 21 24 | |
| AG8 | +VDD_CORE60 | +3.3V_1 | AD10 | 450 mA (A01) | |
| AG9 | +VDD_CORE61 | +3.3V_2 | AE8 | | |
| AH1 | +VDD_CORE62 | +3.3V_3 | AB10 | | |
| AH10 | +VDD_CORE63 | +3.3V_4 | AD9 | | |
| AH11 | +VDD_CORE64 | +3.3V_5 | Y10 | | |
| W26 | +VDD_CORE65 | +3.3V_6 | AB11 | | |
| AH2 | +VDD_CORE66 | +3.3V_7 | AA8 | | |
| AA23 | +VDD_CORE67 | +3.3V_8 | Y9 | | |
| W28 | +VDD_CORE68 | | | | |
| AH25 | +VDD_CORE69 | | | =PP3V3_S5_MCP 8 24 | |
| AH21 | +VDD_CORE70 | +3.3V_DUAL1 | G18 | 16 mA | 266 mA (A01) |
| AH3 | +VDD_CORE71 | +3.3V_DUAL2 | H19 | | |
| AH4 | +VDD_CORE72 | +3.3V_DUAL3 | J20 | | |
| AH5 | +VDD_CORE73 | +3.3V_DUAL4 | K20 | | |
| AH6 | +VDD_CORE74 | | | | |
| AH7 | +VDD_CORE75 | +3.3V_DUAL_USB1 | G26 | 250 mA | |
| AH9 | +VDD_CORE76 | +3.3V_DUAL_USB2 | H27 | | |
| AA24 | +VDD_CORE77 | +3.3V_DUAL_USB3 | J28 | | |
| W21 | +VDD_CORE78 | +3.3V_DUAL_USB4 | K28 | | |
| W23 | +VDD_CORE79 | | | | |
| W25 | +VDD_CORE80 | | | | |
| AF12 | +VDD_CORE81 | | | | |
| | | +VDD_AUXC1 | T21 | =PP1V05_S5_MCP_VDD_AUXC 8 24 | |
| | | +VDD_AUXC2 | U21 | 105 mA (A01) | |
| A20 | +VBAT | +VDD_AUXC3 | V21 | | |

26 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

# MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE | SHT 22 OF 109 | |
| NONE | | |

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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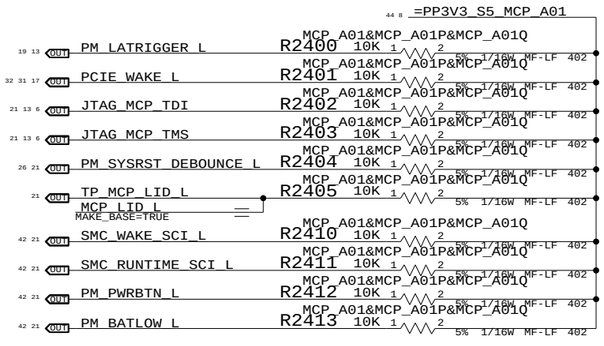
# 3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.


44 8 =PP3V3_S5_MCP_A01
19 13 OUT PM_LATRIGGER_L
R2400 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
32 31 17 OUT PCIE_WAKE_L
R2401 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
21 13 6 OUT JTAG_MCP_TDI
R2402 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
21 13 6 OUT JTAG_MCP_TMS
R2403 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
26 21 OUT PM_SYSRST_DEBOUNCE_L
R2404 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
21 OUT TP_MCP_LID_L
MCP_LID_L
MAKE_BASE=TRUE
R2405 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
42 21 OUT SMC_WAKE_SCI_L
R2410 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
42 21 OUT SMC_RUNTIME_SCI_L
R2411 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
42 21 OUT PM_PWRBTN_L
R2412 10K 1 2 5% 1/16W MF-LF 402
MCP_A01&MCP_A01P&MCP_A01Q
42 21 OUT PM_BATLOW_L
R2413 10K 1 2 5% 1/16W MF-LF 402

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 24 OF 109 | |

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## MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 20% 10V X5R 402-1
C2505 1UF 20% 10V X5R 402-1
C2506 1UF 20% 10V X5R 402-1
C2507 1UF 20% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

## MCP PCIE (DVDD) Power

=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 20% 10V X5R 402-1
C2517 1UF 20% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

## MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

## MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

## MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

## MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

=PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

## MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

## MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

=PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

## MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

## MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

## =PP1V05_ENET_MCP_PLL_MAC

5 mA (A01)

L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

## MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/10W MF-LF 402
R2590 1.47K 1% 1/10W MF-LF 402
MCP_MII_VREF (OUT)
C2591 0.1UF 20% 10V CERM 402

## MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

## =PP3V3_S0_MCP_PLL_UF

19 mA (A01)

L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

## =PP1V05_S0_MCP_AVDD_UF

333 mA (A01)

L2570 30-OHM-5A 0603
PP1V05_S0_MCP_PEX_AVDD: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
206 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603
PP1V05_S0_MCP_SATA_AVDD: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
127 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

## =PP1V05_S0_MCP_PLL_UF

562 mA (A01)

R2580 0.2 1% 1/6W MF 402-HF
PP1V05_S0_MCP_PLL_FSB: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 6.3V CERM 402-LF

L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV: MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

# MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008


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| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 25 | 109 |

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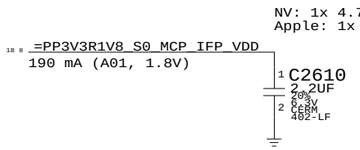
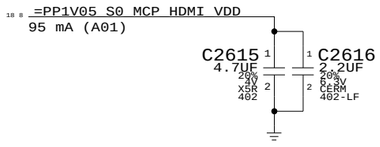
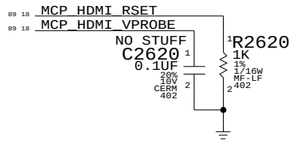
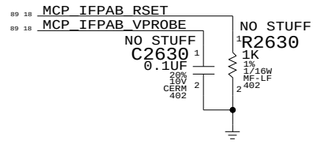
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



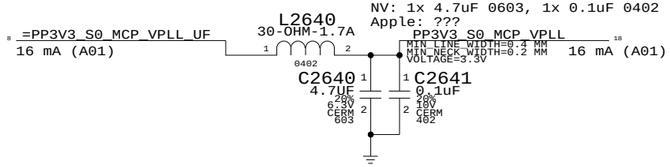



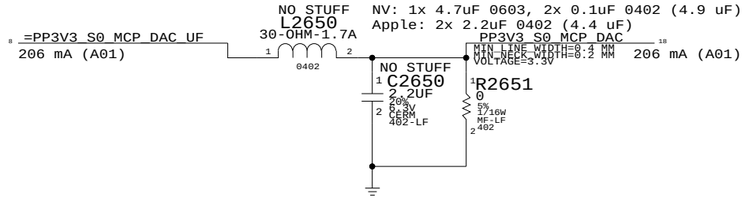




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

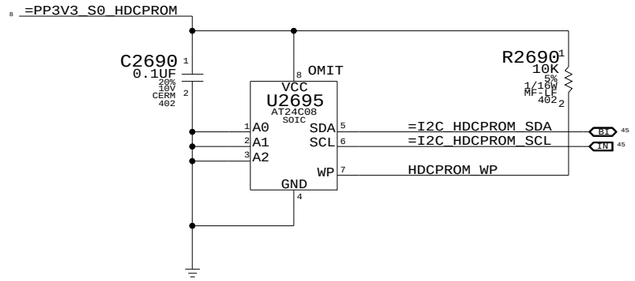
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???




## HDCP ROM

WF: Open question on which packge option(s) nVidia can support.




| | | | |
|---|---|---|---|
| 18 | TP_MCP_RGB_RED | NC_MCP_RGB_RED | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_GREEN | NC_MCP_RGB_GREEN | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_BLUE | NC_MCP_RGB_BLUE | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_HSYNC | NC_MCP_RGB_HSYNC | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_VSYNC | NC_MCP_RGB_VSYNC | MAKE_BASE=TRUE |
| 89 18 | CRT_IG_R_C_PR | NC_CRT_IG_R_C_PR | MAKE_BASE=TRUE |
| 89 18 | CRT_IG_G_Y_Y | NC_CRT_IG_G_Y_Y | MAKE_BASE=TRUE |
| 89 18 | CRT_IG_B_COMP_PB | NC_CRT_IG_B_COMP_PB | MAKE_BASE=TRUE |
| 89 18 | CRT_IG_HSYNC | NC_CRT_IG_HSYNC | MAKE_BASE=TRUE |
| 89 18 | CRT_IG_VSYNC | NC_CRT_IG_VSYNC | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_DAC_RSET | NC_MCP_RGB_DAC_RSET | MAKE_BASE=TRUE |
| 18 | TP_MCP_RGB_DAC_VREF | NC_MCP_RGB_DAC_VREF | MAKE_BASE=TRUE |
| 89 18 | MCP_TV_DAC_RSET | NC_MCP_TV_DAC_RSET | MAKE_BASE=TRUE |
| 89 18 | MCP_TV_DAC_VREF | NC_MCP_TV_DAC_VREF | MAKE_BASE=TRUE |
| 18 | MCP_CLK27M_XTALIN | NC_MCP_CLK27M_XTALIN | MAKE_BASE=TRUE |
| 18 | MCP_CLK27M_XTALOUT | NC_MCP_CLK27M_XTALOUT | MAKE_BASE=TRUE |

# MCP Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008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| SCALE: NONE | SHT 26 OF 109 | |

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

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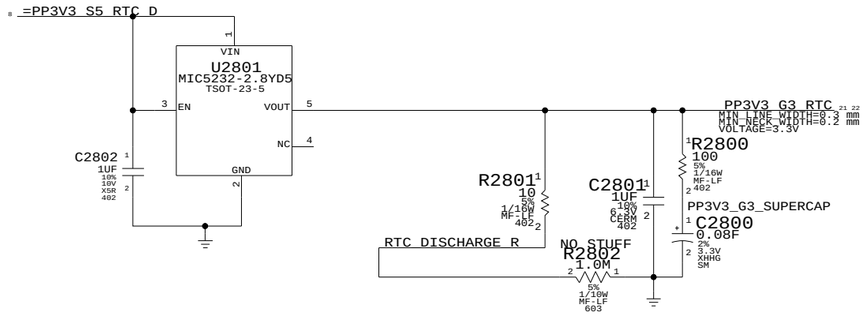
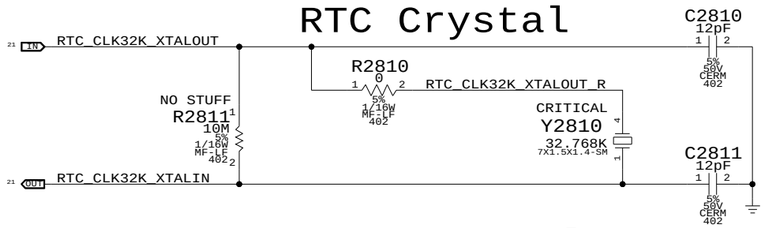
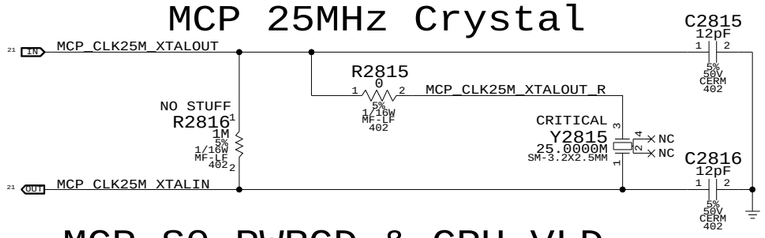
# RTC Power Sources



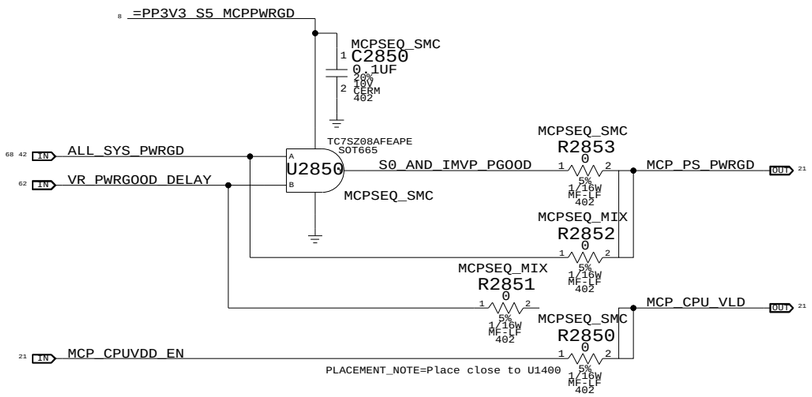

# RTC Crystal




# MCP 25MHz Crystal




# MCP S0 PWRGD & CPU_VLD




MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

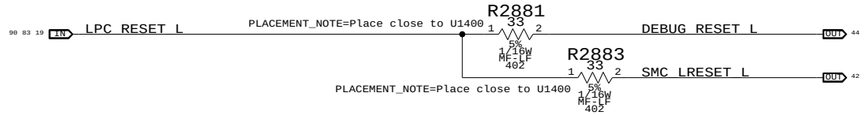
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

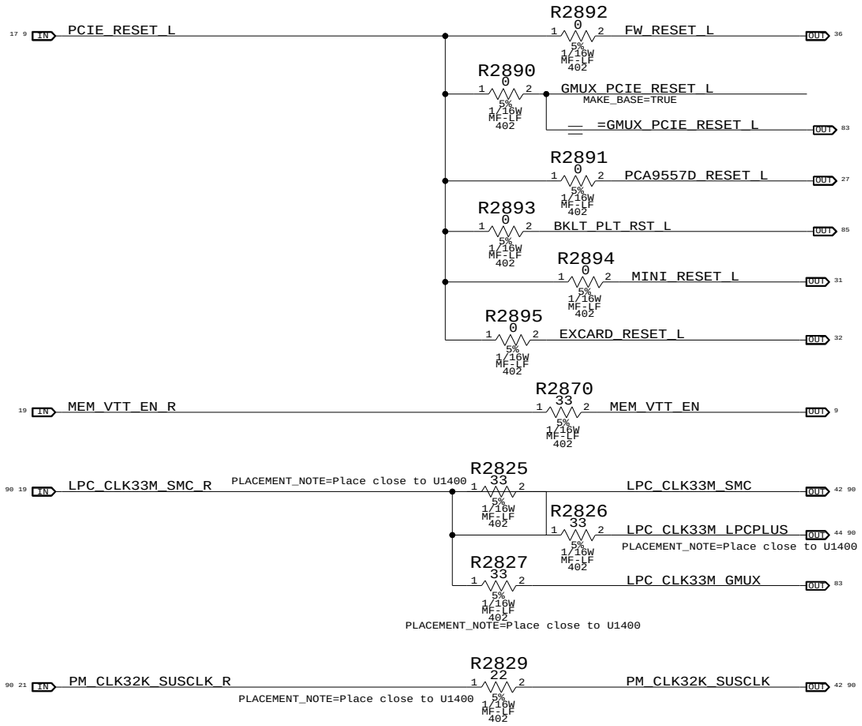
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

# Platform Reset Connections

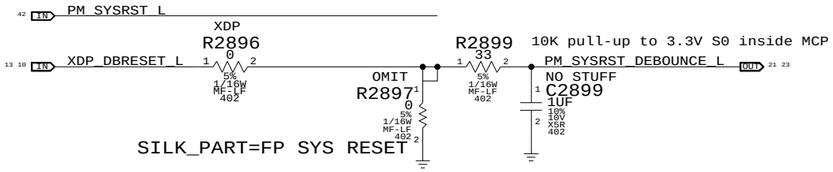
## LPC Reset (Unbuffered)




## PCIE Reset (Unbuffered)




# Reset Button




| SB Misc | | |
|---|---|---|
| SYNC_MASTER=T18_MLB | SYNC_DATE=12/17/2007 | |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| | SCALE: NONE | SHT 28 OF 109 | |

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# Page Notes

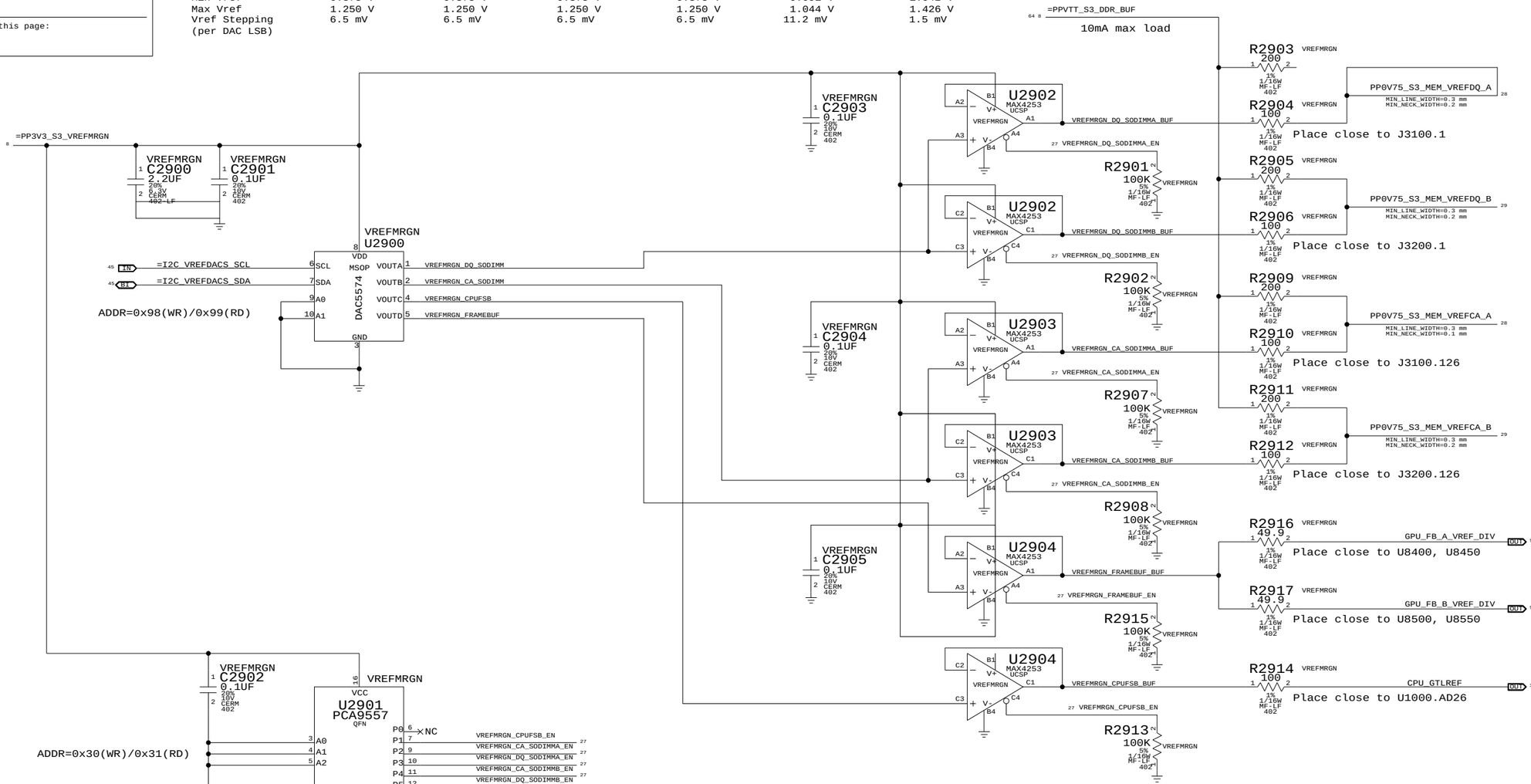
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

| | MEM A VREF DQ | MEM A VREF CA | MEM B VREF DQ | MEM B VREF CA | CPU FSB VREF | FRAME BUFFER VREF |
|---|---|---|---|---|---|---|
| DAC channel | A | B | A | B | C | D |
| Min DAC code | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| Max DAC code | 0x87 | 0x87 | 0x87 | 0x87 | 0x55 | 0xFF |
| Max sink I | -3.75 mA | -3.75 mA | -3.75 mA | -3.75 mA | -0.91 mA | -59.04 mA |
| Max source I | 5 mA | 5 mA | 5 mA | 5 mA | 0.52 mA | 51.15 mA |
| Nominal Vref | 0.75 V | 0.75 V | 0.75 V | 0.75 V | 0.70 V | 1.248 V |
| Min Vref | 0.375 V | 0.375 V | 0.375 V | 0.375 V | 0.091 V | 1.042 V |
| Max Vref | 1.250 V | 1.250 V | 1.250 V | 1.250 V | 1.044 V | 1.426 V |
| Vref Stepping (per DAC LSB) | 6.5 mV | 6.5 mV | 6.5 mV | 6.5 mV | 11.2 mV | 1.5 mV |

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.




Required zero ohm resistors when no VREF margining circuit stuffed

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2903 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2905 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2909 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2911 | CRITICAL | NO_VREFMRGN |

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008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| SCALE: NONE | SHT 29 OF 109 | |

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# DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

## Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

8 =PP1V5_S0_MEM_A

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

27 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

### J3100 (DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2), F-RT-THB)

| | | | |
|---|---|---|---|
| 73 | CKE0 | CKE1 | 74 |
| 75 | VDD | VDD | 76 |
| 77 | NC | A15 | 78 |
| 79 | BA2 | A14 | 80 |
| 81 | VDD | VDD | 82 |
| 83 | A12/BC* | A11 | 84 |
| 85 | A9 | A7 | 86 |
| 87 | VDD | VDD | 88 |
| 89 | A8 | A6 | 90 |
| 91 | A5 | A4 | 92 |
| 93 | VDD | VDD | 94 |
| 95 | A3 | A2 | 96 |
| 97 | A1 | A0 | 98 |
| 99 | VDD | VDD | 100 |
| 101 | CK0 | CK1 | 102 |
| 103 | CK0* | CK1* | 104 |
| 105 | VDD | VDD | 106 |
| 107 | A10/AP | BA1 | 108 |
| 109 | BA0 | RAS* | 110 |
| 111 | VDD | VDD | 112 |
| 113 | WE* | S0* | 114 |
| 115 | CAS* | ODT0 | 116 |
| 117 | VDD | VDD | 118 |
| 119 | A13 | ODT1 | 120 |
| 121 | S1* | NC | 122 |
| 123 | VDD | VDD | 124 |
| 125 | TEST | VREFCA | 126 |
| 127 | VSS | VSS | 128 |
| 129 | DQ32 | DQ36 | 130 |
| 131 | DQ33 | DQ37 | 132 |
| 133 | VSS | VSS | 134 |
| 135 | DQS4* | DM4 | 136 |
| 137 | DQS4 | VSS | 138 |
| 139 | VSS | DQ38 | 140 |
| 141 | DQ34 | DQ39 | 142 |
| 143 | DQ35 | VSS | 144 |
| 145 | VSS | DQ44 | 146 |
| 147 | DQ40 | DQ45 | 148 |
| 149 | DQ41 | VSS | 150 |
| 151 | VSS | DQS5* | 152 |
| 153 | DM5 | DQS5 | 154 |
| 155 | VSS | VSS | 156 |
| 157 | DQ42 | DQ46 | 158 |
| 159 | DQ43 | DQ47 | 160 |
| 161 | VSS | VSS | 162 |
| 163 | DQ48 | DQ52 | 164 |
| 165 | DQ49 | DQ53 | 166 |
| 167 | VSS | VSS | 168 |
| 169 | DQS6* | DM6 | 170 |
| 171 | DQS6 | VSS | 172 |
| 173 | VSS | DQ54 | 174 |
| 175 | DQ50 | DQ55 | 176 |
| 177 | DQ51 | VSS | 178 |
| 179 | VSS | DQ60 | 180 |
| 181 | DQ56 | DQ61 | 182 |
| 183 | DQ57 | VSS | 184 |
| 185 | VSS | DQS7* | 186 |
| 187 | DM7 | DQS7 | 188 |
| 189 | VSS | VSS | 190 |
| 191 | DQ58 | DQ62 | 192 |
| 193 | DQ59 | DQ63 | 194 |
| 195 | VSS | VSS | 196 |
| 197 | SA0 | EVENT* | 198 |
| 199 | VDDSPD | SDA | 200 |
| 201 | SA1 | SCL | 202 |
| 203 | VTT | VTT | 204 |

KEY

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

| | | | |
|---|---|---|---|
| MEM_A_CKE<0> | | MEM_A_CKE<1> | |
| MEM_A_BA<2> | | MEM_A_A<15> | 9 |
| MEM_A_A<12> | | MEM_A_A<14> | |
| MEM_A_A<9> | | MEM_A_A<11> | |
| MEM_A_A<8> | | MEM_A_A<7> | |
| MEM_A_A<5> | | MEM_A_A<6> | |
| MEM_A_A<3> | | MEM_A_A<4> | |
| MEM_A_A<1> | | MEM_A_A<2> | |
| MEM_A_CLK_P<0> | | MEM_A_A<0> | |
| MEM_A_CLK_N<0> | | MEM_A_CLK_P<1> | |
| MEM_A_A<10> | | MEM_A_CLK_N<1> | |
| MEM_A_BA<0> | | MEM_A_BA<1> | |
| MEM_A_WE_L | | MEM_A_RAS_L | |
| MEM_A_CAS_L | | MEM_A_CS_L<0> | |
| MEM_A_A<13> | | MEM_A_ODT<0> | |
| MEM_A_CS_L<1> | | MEM_A_ODT<1> | |
| MEM_A_DQ<33> | | MEM_A_DQ<36> | |
| MEM_A_DQ<32> | | MEM_A_DQ<37> | |
| MEM_A_DQS_N<4> | | MEM_A_DM<4> | |
| MEM_A_DQS_P<4> | | MEM_A_DQ<38> | |
| MEM_A_DQ<34> | | MEM_A_DQ<39> | |
| MEM_A_DQ<35> | | MEM_A_DQ<47> | |
| MEM_A_DQ<44> | | MEM_A_DQ<40> | |
| MEM_A_DQ<41> | | MEM_A_DQS_N<5> | |
| MEM_A_DM<5> | | MEM_A_DQS_P<5> | |
| MEM_A_DQ<45> | | MEM_A_DQ<46> | |
| MEM_A_DQ<42> | | MEM_A_DQ<43> | |
| MEM_A_DQ<52> | | MEM_A_DQ<48> | |
| MEM_A_DQ<51> | | MEM_A_DQ<53> | |
| MEM_A_DQS_N<6> | | MEM_A_DM<6> | |
| MEM_A_DQS_P<6> | | MEM_A_DQ<50> | |
| MEM_A_DQ<55> | | MEM_A_DQ<49> | |
| MEM_A_DQ<54> | | MEM_A_DQ<57> | |
| MEM_A_DQ<61> | | MEM_A_DQ<56> | |
| MEM_A_DQ<60> | | MEM_A_DQS_N<7> | |
| MEM_A_DM<7> | | MEM_A_DQS_P<7> | |
| MEM_A_DQ<58> | | MEM_A_DQ<62> | |
| MEM_A_DQ<59> | | MEM_A_DQ<63> | |
| MEM_A_SA<0> | | MEM_EVENT_L | 21 29 42 |
| MEM_A_SA<1> | | =I2C_SODIMMA_SDA | 45 |
| | | =I2C_SODIMMA_SCL | 45 |
| | | =PP0V75_S0_MEM_VTT_A | 8 |

8 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

### J3100 (DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2), CRITICAL, F-RT-THB)

| | | | |
|---|---|---|---|
| 1 | VREFDQ | VSS | 2 |
| 3 | VSS | DQ4 | 4 |
| 5 | DQ0 | DQ5 | 6 |
| 7 | DQ1 | VSS | 8 |
| 9 | VSS | DQS0* | 10 |
| 11 | DM0 | DQS0 | 12 |
| 13 | VSS | VSS | 14 |
| 15 | DQ2 | DQ6 | 16 |
| 17 | DQ3 | DQ7 | 18 |
| 19 | VSS | VSS | 20 |
| 21 | DQ8 | DQ12 | 22 |
| 23 | DQ9 | DQ13 | 24 |
| 25 | VSS | VSS | 26 |
| 27 | DQS1* | DM1 | 28 |
| 29 | DQS1 | RESET* | 30 |
| 31 | VSS | VSS | 32 |
| 33 | DQ10 | DQ14 | 34 |
| 35 | DQ11 | DQ15 | 36 |
| 37 | VSS | VSS | 38 |
| 39 | DQ16 | DQ20 | 40 |
| 41 | DQ17 | DQ21 | 42 |
| 43 | VSS | VSS | 44 |
| 45 | DQS2* | DM2 | 46 |
| 47 | DQS2 | VSS | 48 |
| 49 | VSS | DQ22 | 50 |
| 51 | DQ18 | DQ23 | 52 |
| 53 | DQ19 | VSS | 54 |
| 55 | VSS | DQ28 | 56 |
| 57 | DQ24 | DQ29 | 58 |
| 59 | DQ25 | VSS | 60 |
| 61 | VSS | DQS3* | 62 |
| 63 | DM3 | DQS3 | 64 |
| 65 | VSS | VSS | 66 |
| 67 | DQ26 | DQ30 | 68 |
| 69 | DQ27 | DQ31 | 70 |
| 71 | VSS | VSS | 72 |

KEY

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

516-0201

| | | | |
|---|---|---|---|
| MEM_A_DQ<0> | | MEM_A_DQ<4> | |
| MEM_A_DQ<1> | | MEM_A_DQ<5> | |
| MEM_A_DM<0> | | MEM_A_DQS_N<0> | |
| MEM_A_DQ<3> | | MEM_A_DQS_P<0> | |
| MEM_A_DQ<2> | | MEM_A_DQ<6> | |
| MEM_A_DQ<9> | | MEM_A_DQ<7> | |
| MEM_A_DQ<13> | | MEM_A_DQ<8> | |
| MEM_A_DQS_N<1> | | MEM_A_DQ<12> | |
| MEM_A_DQS_P<1> | | MEM_A_DM<1> | |
| MEM_A_DQ<11> | | MEM_RESET_L | 29 30 |
| MEM_A_DQ<14> | | MEM_A_DQ<15> | |
| MEM_A_DQ<16> | | MEM_A_DQ<10> | |
| MEM_A_DQ<18> | | MEM_A_DQ<21> | |
| MEM_A_DQS_N<2> | | MEM_A_DQ<20> | |
| MEM_A_DQS_P<2> | | MEM_A_DM<2> | |
| MEM_A_DQ<23> | | MEM_A_DQ<17> | |
| MEM_A_DQ<19> | | MEM_A_DQ<22> | |
| MEM_A_DQ<24> | | MEM_A_DQ<29> | |
| MEM_A_DQ<30> | | MEM_A_DQ<28> | |
| MEM_A_DM<3> | | MEM_A_DQS_N<3> | |
| MEM_A_DQ<27> | | MEM_A_DQS_P<3> | |
| MEM_A_DQ<25> | | MEM_A_DQ<26> | |
| | | MEM_A_DQ<31> | |

PP0V75_S3_MEM_VREFCA_A 27

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 31 OF 109 | |

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# DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

## Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

8 =PP1V5_S0_MEM_B

8 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603

C3210 C3211 C3212 C3213 C3214 C3215 C3216 C3217 C3218 C3219 C3220 C3221 C3222 C3223
0.1UF 20% 10V CERM 402

27 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 88 15 IN | MEM_B_CKE<0> | 73 | CKE0 | CKE1 | 74 | MEM_B_CKE<1> | IN 15 88 |
| | | 75 | VDD | VDD | 76 | | |
| | | 77 | NC | A15 | 78 | MEM_B_A<15> | IN 9 |
| 88 15 IN | MEM_B_BA<2> | 79 | BA2 | A14 | 80 | MEM_B_A<14> | IN 15 88 |
| | | 81 | VDD | VDD | 82 | | |
| 88 15 IN | MEM_B_A<12> | 83 | A12/BC* | A11 | 84 | MEM_B_A<11> | IN 15 88 |
| 88 15 IN | MEM_B_A<9> | 85 | A9 | A7 | 86 | MEM_B_A<7> | IN 15 88 |
| | | 87 | VDD | VDD | 88 | | |
| 88 15 IN | MEM_B_A<8> | 89 | A8 | A6 | 90 | MEM_B_A<6> | IN 15 88 |
| 88 15 IN | MEM_B_A<5> | 91 | A5 | A4 | 92 | MEM_B_A<4> | IN 15 88 |
| | | 93 | VDD | VDD | 94 | | |
| 88 15 IN | MEM_B_A<3> | 95 | A3 | A2 | 96 | MEM_B_A<2> | IN 15 88 |
| 88 15 IN | MEM_B_A<1> | 97 | A1 | A0 | 98 | MEM_B_A<0> | IN 15 88 |
| | | 99 | VDD | VDD | 100 | | |
| 88 15 IN | MEM_B_CLK_P<0> | 101 | CK0 | CK1 | 102 | MEM_B_CLK_P<1> | IN 15 88 |
| 88 15 IN | MEM_B_CLK_N<0> | 103 | CK0* | CK1* | 104 | MEM_B_CLK_N<1> | IN 15 88 |
| | | 105 | VDD | VDD | 106 | | |
| 88 15 IN | MEM_B_A<10> | 107 | A10/AP | BA1 | 108 | MEM_B_BA<1> | IN 15 88 |
| 88 15 IN | MEM_B_BA<0> | 109 | BA0 | RAS* | 110 | MEM_B_RAS_L | IN 15 88 |
| | | 111 | VDD | VDD | 112 | | |
| 88 15 IN | MEM_B_WE_L | 113 | WE* | S0* | 114 | MEM_B_CS_L<0> | IN 15 88 |
| 88 15 IN | MEM_B_CAS_L | 115 | CAS* | ODT0 | 116 | MEM_B_ODT<0> | IN 15 88 |
| | | 117 | VDD | VDD | 118 | | |
| 88 15 IN | MEM_B_A<13> | 119 | A13 | ODT1 | 120 | MEM_B_ODT<1> | IN 15 88 |
| 88 15 IN | MEM_B_CS_L<1> | 121 | S1* | NC | 122 | | |
| | | 123 | VDD | VDD | 124 | | |
| | | 125 | TEST | VREFCA | 126 | | |
| | | 127 | VSS | VSS | 128 | | |
| 88 15 BI | MEM_B_DQ<32> | 129 | DQ32 | DQ36 | 130 | MEM_B_DQ<33> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<37> | 131 | DQ33 | DQ37 | 132 | MEM_B_DQ<36> | BI 15 88 |
| | | 133 | VSS | VSS | 134 | | |
| 88 15 BI | MEM_B_DQS_N<4> | 135 | DQS4* | DM4 | 136 | MEM_B_DM<4> | IN 15 88 |
| 88 15 BI | MEM_B_DQS_P<4> | 137 | DQS4 | VSS | 138 | | |
| | | 139 | VSS | DQ38 | 140 | MEM_B_DQ<38> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<34> | 141 | DQ34 | DQ39 | 142 | MEM_B_DQ<39> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<35> | 143 | DQ35 | VSS | 144 | | |
| | | 145 | VSS | DQ44 | 146 | MEM_B_DQ<44> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<41> | 147 | DQ40 | DQ45 | 148 | MEM_B_DQ<45> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<40> | 149 | DQ41 | VSS | 150 | | |
| | | 151 | VSS | DQS5* | 152 | MEM_B_DQS_N<5> | BI 15 88 |
| 88 15 IN | MEM_B_DM<5> | 153 | DM5 | DQS5 | 154 | MEM_B_DQS_P<5> | BI 15 88 |
| | | 155 | VSS | VSS | 156 | | |
| 88 15 BI | MEM_B_DQ<43> | 157 | DQ42 | DQ46 | 158 | MEM_B_DQ<47> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<42> | 159 | DQ43 | DQ47 | 160 | MEM_B_DQ<46> | BI 15 88 |
| | | 161 | VSS | VSS | 162 | | |
| 88 15 BI | MEM_B_DQ<55> | 163 | DQ48 | DQ52 | 164 | MEM_B_DQ<48> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<49> | 165 | DQ49 | DQ53 | 166 | MEM_B_DQ<54> | BI 15 88 |
| | | 167 | VSS | VSS | 168 | | |
| 88 15 BI | MEM_B_DQS_N<6> | 169 | DQS6* | DM6 | 170 | MEM_B_DM<6> | IN 15 88 |
| 88 15 BI | MEM_B_DQS_P<6> | 171 | DQS6 | VSS | 172 | | |
| | | 173 | VSS | DQ54 | 174 | MEM_B_DQ<53> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<52> | 175 | DQ50 | DQ55 | 176 | MEM_B_DQ<50> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<51> | 177 | DQ51 | VSS | 178 | | |
| | | 179 | VSS | DQ60 | 180 | MEM_B_DQ<60> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<56> | 181 | DQ56 | DQ61 | 182 | MEM_B_DQ<61> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<57> | 183 | DQ57 | VSS | 184 | | |
| | | 185 | VSS | DQS7* | 186 | MEM_B_DQS_N<7> | BI 15 88 |
| 88 15 IN | MEM_B_DM<7> | 187 | DM7 | DQS7 | 188 | MEM_B_DQS_P<7> | BI 15 88 |
| | | 189 | VSS | VSS | 190 | | |
| 88 15 BI | MEM_B_DQ<63> | 191 | DQ58 | DQ62 | 192 | MEM_B_DQ<58> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<59> | 193 | DQ59 | DQ63 | 194 | MEM_B_DQ<62> | BI 15 88 |
| | | 195 | VSS | VSS | 196 | | |
| | MEM_B_SA<0> | 197 | SA0 | EVENT* | 198 | MEM_EVENT_L | OUT 21 28 42 |
| | | 199 | VDDSPD | SDA | 200 | =I2C_SODIMMB_SDA | BI 45 |
| | MEM_B_SA<1> | 201 | SA1 | SCL | 202 | =I2C_SODIMMB_SCL | IN 45 |
| | | 203 | VTT | VTT | 204 | =PP0V75_S0_MEM_VTT_B | 8 |
| | | MTG PINS | | | | | |
| | | 205 | MTG PIN | MTG PIN | 206 | | |
| | | 207 | MTG PIN | MTG PIN | 208 | | |
| | | 209 | MTG PIN | MTG PIN | 210 | | |
| | | 211 | MTG PIN | MTG PIN | 212 | | |

KEY

516s0706

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402

8 =PPSPD_S0_MEM_B

C3240 2.2UF 20% 6.3V CERM 402-LF

J3200 CRITICAL F-RT-BGA3 DDR3-SODIMM (1 OF 2)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | 1 | VREFDQ | VSS | 2 | | |
| 88 15 BI | MEM_B_DQ<0> | 3 | VSS | DQ4 | 4 | MEM_B_DQ<4> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<1> | 5 | DQ0 | DQ5 | 6 | MEM_B_DQ<5> | BI 15 88 |
| | | 7 | DQ1 | VSS | 8 | | |
| 88 15 IN | MEM_B_DM<0> | 9 | VSS | DQS0* | 10 | MEM_B_DQS_N<0> | BI 15 88 |
| | | 11 | DM0 | DQS0 | 12 | MEM_B_DQS_P<0> | BI 15 88 |
| | | 13 | VSS | VSS | 14 | | |
| 88 15 BI | MEM_B_DQ<2> | 15 | DQ2 | DQ6 | 16 | MEM_B_DQ<6> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<3> | 17 | DQ3 | DQ7 | 18 | MEM_B_DQ<7> | BI 15 88 |
| | | 19 | VSS | VSS | 20 | | |
| 88 15 BI | MEM_B_DQ<28> | 21 | DQ8 | DQ12 | 22 | MEM_B_DQ<29> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<24> | 23 | DQ9 | DQ13 | 24 | MEM_B_DQ<25> | BI 15 88 |
| | | 25 | VSS | VSS | 26 | | |
| 88 15 BI | MEM_B_DQS_N<3> | 27 | DQS1* | DM1 | 28 | MEM_B_DM<3> | IN 15 88 |
| 88 15 BI | MEM_B_DQS_P<3> | 29 | DQS1 | RESET* | 30 | MEM_RESET_L | IN 28 30 |
| | | 31 | VSS | VSS | 32 | | |
| 88 15 BI | MEM_B_DQ<31> | 33 | DQ10 | DQ14 | 34 | MEM_B_DQ<26> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<30> | 35 | DQ11 | DQ15 | 36 | MEM_B_DQ<27> | BI 15 88 |
| | | 37 | VSS | VSS | 38 | | |
| 88 15 BI | MEM_B_DQ<9> | 39 | DQ16 | DQ20 | 40 | MEM_B_DQ<13> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<8> | 41 | DQ17 | DQ21 | 42 | MEM_B_DQ<12> | BI 15 88 |
| | | 43 | VSS | VSS | 44 | | |
| 88 15 BI | MEM_B_DQS_N<1> | 45 | DQS2* | DM2 | 46 | MEM_B_DM<1> | IN 15 88 |
| 88 15 BI | MEM_B_DQS_P<1> | 47 | DQS2 | VSS | 48 | | |
| | | 49 | VSS | DQ22 | 50 | MEM_B_DQ<14> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<15> | 51 | DQ18 | DQ23 | 52 | MEM_B_DQ<11> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<10> | 53 | DQ19 | VSS | 54 | | |
| | | 55 | VSS | DQ28 | 56 | MEM_B_DQ<20> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<21> | 57 | DQ24 | DQ29 | 58 | MEM_B_DQ<16> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<17> | 59 | DQ25 | VSS | 60 | | |
| | | 61 | VSS | DQS3* | 62 | MEM_B_DQS_N<2> | BI 15 88 |
| 88 15 IN | MEM_B_DM<2> | 63 | DM3 | DQS3 | 64 | MEM_B_DQS_P<2> | BI 15 88 |
| | | 65 | VSS | VSS | 66 | | |
| 88 15 BI | MEM_B_DQ<18> | 67 | DQ26 | DQ30 | 68 | MEM_B_DQ<19> | BI 15 88 |
| 88 15 BI | MEM_B_DQ<22> | 69 | DQ27 | DQ31 | 70 | MEM_B_DQ<23> | BI 15 88 |
| | | 71 | VSS | VSS | 72 | | |

KEY

516s0706

PP0V75_S3_MEM_VREFCA_B 27

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 32 OF 109 | |

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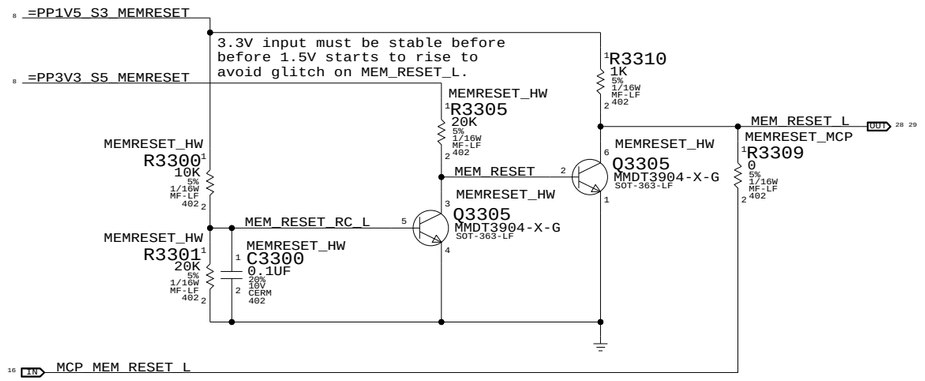
# DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.




## DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008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APPLE INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE | SHT | OF |
| NONE | 33 | 109 |

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PCIE_MINI_PRSNT_L

Q3401
SSM6N15FEAPE
SOT563

AP_PWR_EN

MINI_CLKREQ_L

Q3401
SSM6N15FEAPE
SOT563

## 5V S3 WLAN FET

| | |
|---|---|
| MOSFET | FDC606P |
| CHANNEL | P-TYPE |
| RDS(ON) | 26 mOhm @4.5V |
| LOADING | 0.8 A (EDP) |

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
NC
NC

PLACEMENT_NOTE=Place close to J3401.

C3431 0.1uF 10% 16V X5R 402
C3430 0.1uF 10% 16V X5R 402

PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=Place close to J3401.

# AIRPORT

L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N

PLACEMENT_NOTE=Place close to J3401.

1000 mA peak
750 mA nominal max

L3404
FERR-120-OHM-1.5A
0402-LF

PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

C3422 1uF 10% 10V CERM 402
C3421 0.1uF 10% 10V CERM 402
C3420 10UF 20% 10V X5R 805

PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
PLACEMENT_NOTE=Place close to Q3450.

Q3450
FDC606P_G
SOT-6

PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

C3450 0.1UF 10% 10V X5R 402
P5VWLAN_SS

C3451 0.033UF 10% 16V X5R 402
R3450 100K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402

=PP5V_S3_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PM_WLAN_EN_L

275 mA peak
206 mA nominal max

L3405
FERR-120-OHM-1.5A
0402-LF

C3452 0.1UF 10% 10V CERM 402

PP5V_S3_BTCAMERA_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

I2C_ALS_SDA
I2C_ALS_SCL

# ALS CAMERA

USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

L3402
90-OHM
DLP0NS

USB_CAMERA_P
USB_CAMERA_N

PLACEMENT_NOTE=Place close to J3401.

CONN_USB2_BT_P
CONN_USB2_BT_N

# BLUETOOTH

L3403
90-OHM
DLP0NS

USB_BT_P
USB_BT_N

PLACEMENT_NOTE=Place close to J3401.

PP5V_WLAN_F

R3453 33K 5% 1/16W MF-LF 402

=PP3V3_S3_WLAN

U3402
74LVC1G17DRL
SOT-553

TC7SZ08AFEAPE
SOT665
U3401

WLAN_SMIT_BUF
WLAN_SMIT_RC

C3453 1UF 10% 6.3V CERM 402

R3454 62K 5% 1/16W MF-LF 402

MINI_RESET_CONN_L
MINI_RESET_L

## Right Clutch Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008


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# EXPRESSCARD/34 FLEX CONNECTOR

## INPUT DECOUPLING

32 8 =PP3V3_S3_EXCARD
C3530 0.1uF 20% 10V CERM 402
C3531 10uF 20% 6.3V X5R 603

32 8 =PP1V5_S0_EXCARD
C3534 0.1uF 20% 10V CERM 402
C3535 10uF 20% 6.3V X5R 603

## L3502

90-OHM DLP0NS SYM_VER-1

90 20 BI USB_EXCARD_N — 4 — 3 — USB2_EXCARD_CONN_N 7 32 95
90 20 BI USB_EXCARD_P — 1 — 2 — USB2_EXCARD_CONN_P 7 32 95

PLACEMENT_NOTE=Place close to J3500

## L3503

90-OHM-100MA DLP11S SYM_VER-1

89 17 IN PCIE_CLK100M_EXCARD_N — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N 7 32 95
89 17 IN PCIE_CLK100M_EXCARD_P — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P 7 32 95

PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500

## C3571

89 17 IN PCIE_EXCARD_R2D_C_N — 1 — 2 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_N 7 32 89 95
89 17 IN PCIE_EXCARD_R2D_C_P — 1 — 2 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P 7 32 89 95

## C3570

PLACEMENT_NOTE=Place close to J3500

CRITICAL

## J3500

502250-8627 F-RT-SM

95 89 32 7 PCIE_EXCARD_R2D_N — 4
89 17 7 OUT PCIE_EXCARD_D2R_P — 6
95 32 7 PCIE_CLK100M_EXCARD_CONN_N — 10
32 7 EXCARD_CLKREQ_CONN_L — 12
32 7 PP3V3_S0_EXCARD_SWITCH — 14
32 7 PP3V3_S3_EXCARD_SWITCH — 16
32 7 PP1V5_S0_EXCARD_SWITCH — 18
40 BI =SMBUS_EXCARD_SDA — 20
NC — 22
32 7 EXCARD_CPUSB_L — 24
95 32 7 USB2_EXCARD_CONN_N — 26

1 — 3 — PCIE_EXCARD_R2D_P 7 32 89 95
5 — 7 — PCIE_EXCARD_D2R_N 7 17 89
9 — PCIE_CLK100M_EXCARD_CONN_P 7 32 95
11 — EXCARD_CPPE_L 7 32
13 — PP3V3_S0_EXCARD_SWITCH 7 32
15 — PLT_RESET_SWITCH_L 7 32
17 — PCIE_WAKE_L 17 23 31
19 — PP1V5_S0_EXCARD_SWITCH 7 32
21 — =SMBUS_EXCARD_SCL BI 45
23 — NC
25 — USB2_EXCARD_CONN_P 7 32 95
27

28 29

32 7 EXCARD_CPPE_L — R3501 0.1 MF-LF 402 2 5% 1/16W — PCIE_EXCARD_PRSNT_L 17

## OUTPUT DECOUPLING

CRITICAL

## U3500

TPS2231 QFN

32 8 =PP3V3_S3_EXCARD
32 8 =PP3V3_S0_EXCARD
32 8 =PP1V5_S0_EXCARD
42 IN SMC_EXCARD_PWR_EN — R3500 0.1 MF-LF 402 2 5% 1/16W — EXCARD_SHDN_L_R
TP_EXCARD_STBY_L
26 IN EXCARD_RESET_L
43 28 IN EXCARD_OC_L

17 AUXIN — AUXOUT 15
2 VIN3P3 — VOUT3P3 3
12 VIN1P5 — VOUT1P5 11
28 SHDN* — PERST* 8
1 STBY* — CPPE* 10
6 SYSRST* — CPUSB* 9
19 OC*
NC 4 NC0 — RCLKEN 18 EXCARD_RCLKEN 32
NC 5 NC1
NC 13 NC2
NC 14 NC3
NC 16 NC4 — THRML_PAD 21
7 GND

PP3V3_S3_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.3mm MIN_NECK_WIDTH=0.2mm
C3500 0.1uF 20% 10V CERM 402
C3503 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3501 0.1uF 20% 10V CERM 402
C3504 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH 7 32
VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3502 0.1uF 20% 10V CERM 402
C3505 10uF 20% 6.3V X5R 603

PLT_RESET_SWITCH_L 7 32
EXCARD_CPPE_L 7 32
EXCARD_CPUSB_L 7 32

VENICE

## C3573

PCIE_FC_R2D_C_P — 1 — 2 0.1uF 10% 16V X5R 402 — PCIE_FC_R2D_P 95
PCIE_FC_R2D_C_N — 1 — 2 0.1uF 10% 16V X5R 402 — PCIE_FC_R2D_N 95

## C3572

PLACEMENT_NOTE=Place close to J3501.

CRITICAL

## J3501

503219-0221 M-ST-SM

9 OUT FC_CLKREQ_L — 1 — 2
95 9 IN PCIE_CLK100M_FC_P — 3 — 4
95 9 IN PCIE_CLK100M_FC_N — 5 — 6
7 — 8 — NC
9 — 10 — =PP3V3_FC_CON 8
11 — 12 — NC
13 — 14 — NC
15 — 16 — =PP1V5_FC_CON 8
95 9 OUT PCIE_FC_D2R_P — 17 — 18 — NC
95 9 OUT PCIE_FC_D2R_N — 19 — 20 — FC_PRSNT_L OUT 9
21 — 22 — FC_RESET_L OUT 9
23 — 24
25 — 26

VENICE

Venice Connector

32 8 =PP3V3_S3_EXCARD
32 7 EXCARD_CPUSB_L
32 7 EXCARD_CPPE_L
U3551 74HC1G00GWDG SC70-5
SMC_EXCARD_CP OUT 42 43
C3550 0.1uF 20% 10V CERM 402

32 8 =PP3V3_S0_EXCARD
R3561 100K 1/16W MF-LF 402
32 7 EXCARD_CLKREQ_CONN_L
U3561 SN74LVC1G04YZPR BGA
C3560 0.1uF 20% 10V CERM 402
32 EXCARD_RCLKEN
EXCARD_CLKREQ_CONN
U3560 74HC1G00GWDG SC70-5
EXCARD_CLKREQ_L OUT 17

ExpressCard Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

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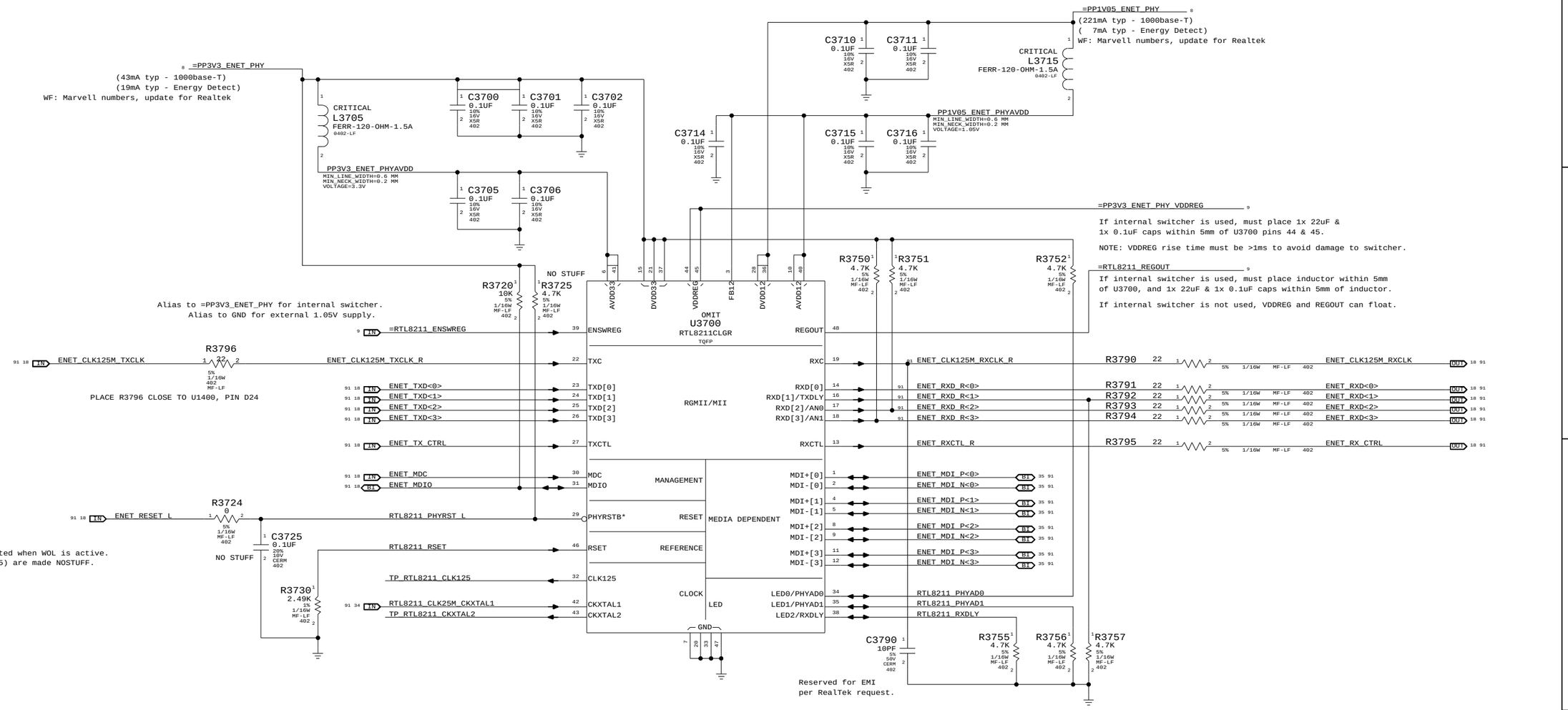


Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

# Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008


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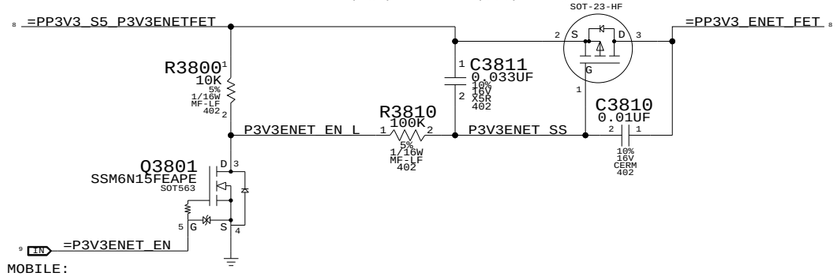
# 3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q3810
NTR4101P
SOT-23-HF



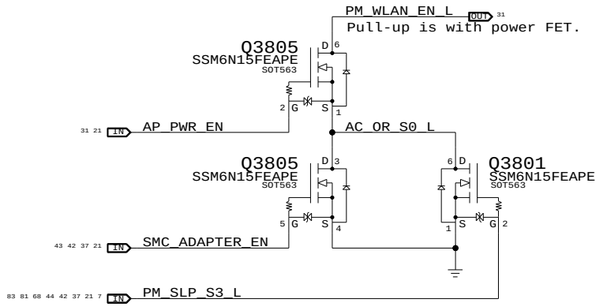

MOBILE:

Recommend aliasing PM_SLP_RMGT_L and
=P3V3ENET_EN. Nets separated on
ARB for alternate power options.

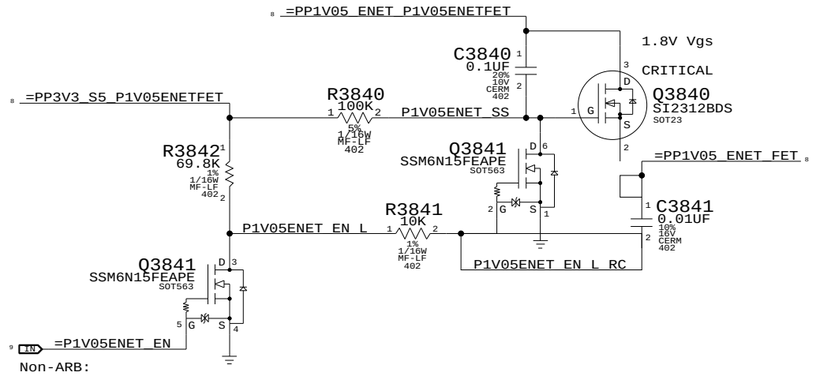
# WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.




# 1.05V ENET FET




Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and
=P1V05ENET_EN. Nets separated on
ARB for alternate power options.

# RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008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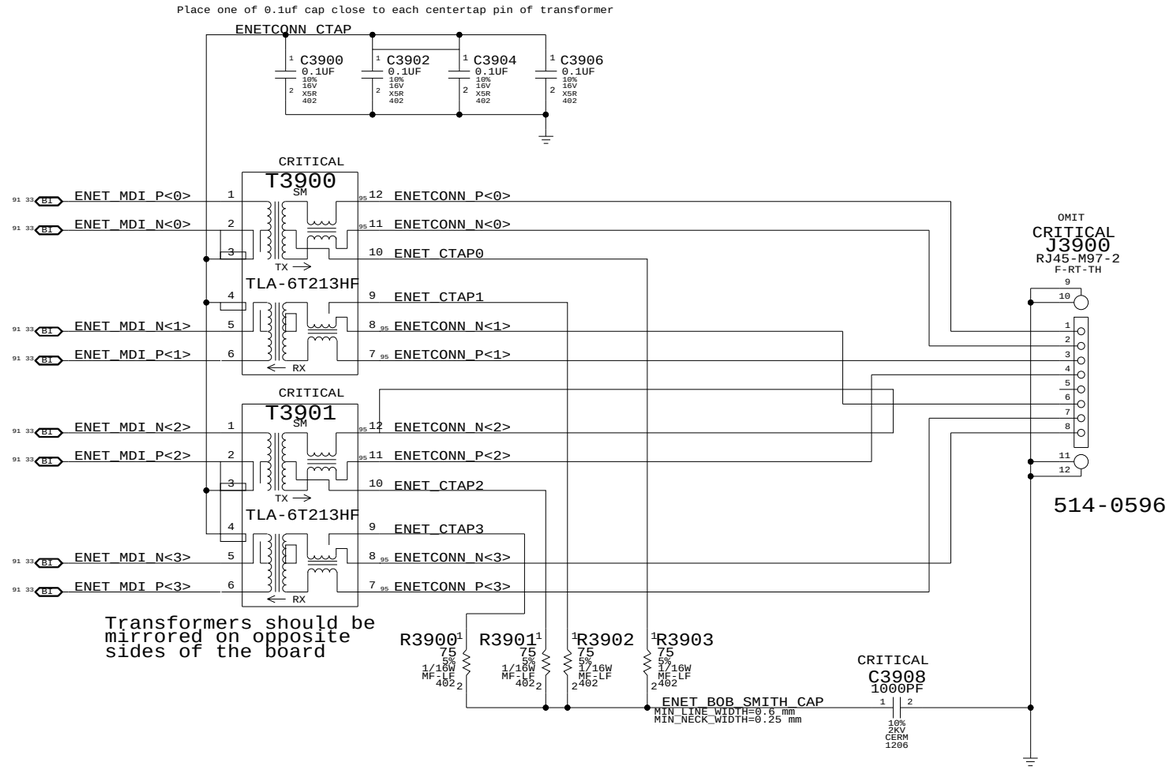
# Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 514-0636 | 1 | CONN,RJ45,HB,10/100TX | J3900 | CRITICAL | |

# Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008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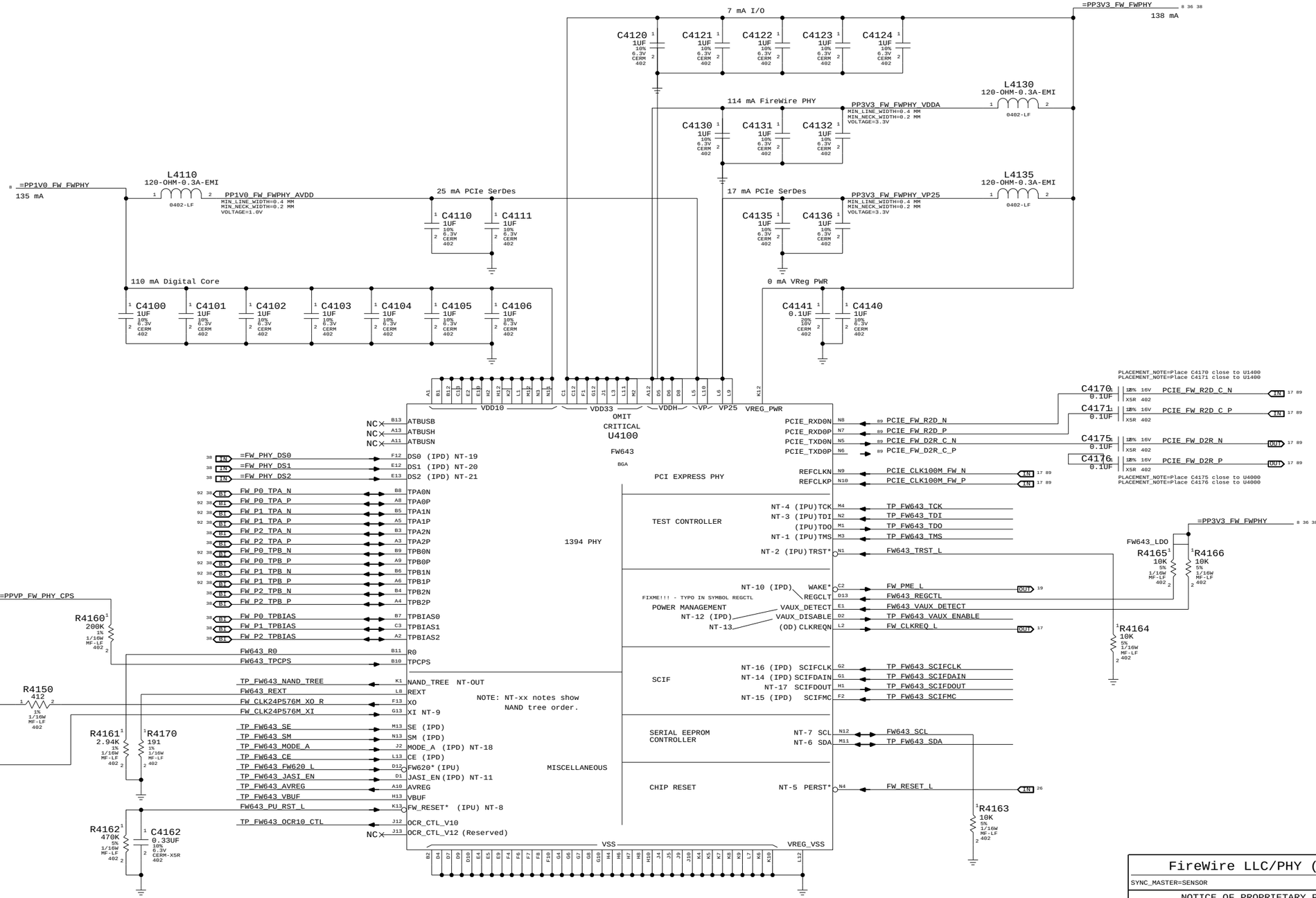


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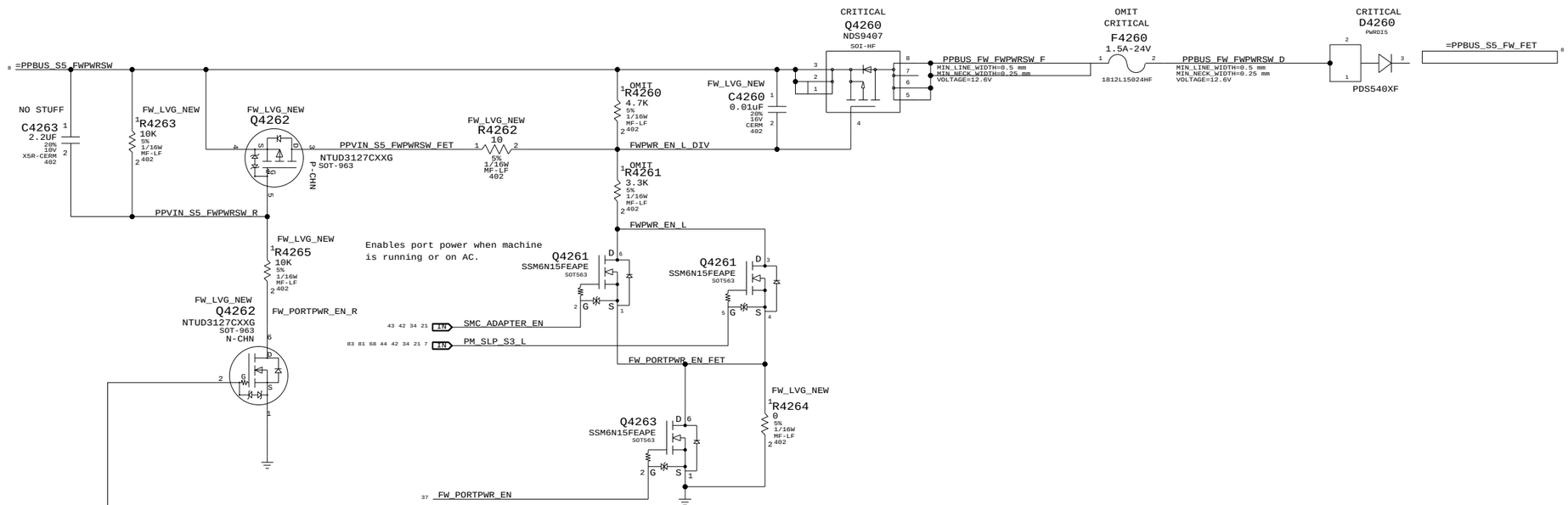
# Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

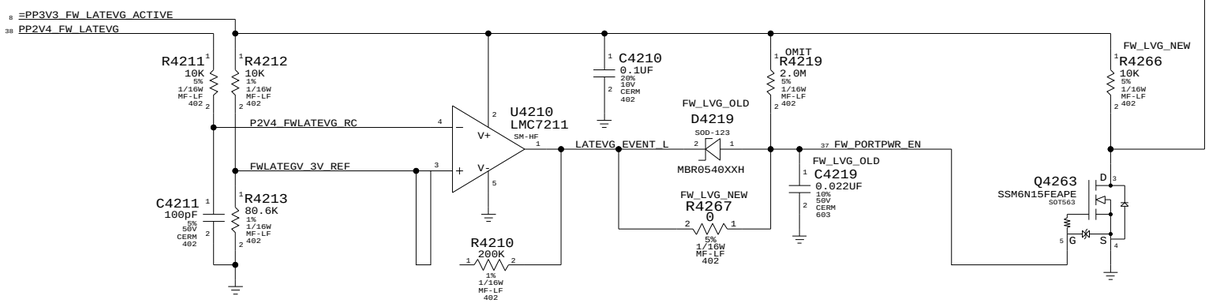
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

## FireWire Port Power Switch




## Late-VG Event Detection




FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 740S0080 | 1 | LITTLEFUSE, 1.5A RESETTABLE 24V | F4260 | CRITICAL | |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 116S0145 | 1 | RES,MTL FILM,2.0M,5%,0402,SM,LF | R4219 | | FW_LVG_OLD |
| 116S0082 | 1 | RES,MTL FILM,4.7K,5%,0402,SM,LF | R4260 | | FW_LVG_OLD |
| 116S0078 | 1 | RES,MTL FILM,3.3K,5%,0402,SM,LF | R4261 | | FW_LVG_OLD |
| 116S0149 | 1 | RES,MTL FILM,10K,5%,0402,SM,LF | R4219 | | FW_LVG_NEW |
| 116S0130 | 1 | RES,MTL FILM,470K,5%,0402,SM,LF | R4260 | | FW_LVG_NEW |
| 116S0126 | 1 | RES,MTL FILM,330K,5%,0402,SM,LF | R4261 | | FW_LVG_NEW |

FireWire Port Power

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008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# Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

# FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

38 36 8 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402
R4380 10K 1% 1/16W MF-LF 402
R4381 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE — =FW_PHY_DS0 (36)
FWPHY_DS2 MAKE_BASE=TRUE — =FW_PHY_DS2 (36)
FWPHY_DS1 MAKE_BASE=TRUE — =FW_PHY_DS1 (36)

36 FW_P0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE
36 FW_P2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE
92 36 FW_P0_TPA_N — NC_FW0_TPAN MAKE_BASE=TRUE
92 36 FW_P0_TPA_P — NC_FW0_TPAP MAKE_BASE=TRUE
36 FW_P2_TPA_N — NC_FW2_TPAN MAKE_BASE=TRUE
36 FW_P2_TPA_P — NC_FW2_TPAP MAKE_BASE=TRUE

92 36 FW_P0_TPB_N — NC_FW0_TPBN MAKE_BASE=TRUE
92 36 FW_P0_TPB_P — NC_FW0_TPBP MAKE_BASE=TRUE
36 FW_P2_TPB_N — NC_FW2_TPBN MAKE_BASE=TRUE
36 FW_P2_TPB_P — NC_FW2_TPBP MAKE_BASE=TRUE

# Termination

Place close to FireWire PHY

36 FW_P1_TPBIAS — TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

92 36 FW_P1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE (38)
92 36 FW_P1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE (38)
92 36 FW_P1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE (38)
92 36 FW_P1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE (38)

SIGNAL_MODEL=EMPTY
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 50V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW SOT-363 (SYM-VER3)

R4311 470K 5% 1/16W MF-LF 402

PPVP_FW_PHY_CPS MAKE_BASE=TRUE — =PPVP_FW_PHY_CPS (36)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

38 36 8 =PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

## "Snapback" & "Late VG" Protection

38 37 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363
DP4311 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

38 FW_PORT1_TPB_N
38 FW_PORT1_TPB_P
38 FW_PORT1_TPA_N
38 FW_PORT1_TPA_P

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

## Cable Power

8 =PPVP_FW_PORT1

CRITICAL
L4310 FERR-250-OHM SM
Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

## PORT 1

BILINGUAL

CRITICAL
J4310 1394B-M97 F-RT-TH

(FW_PORT1_BREF) — OUTPUT
(GND_FW_PORT1_VG) — NC
FW_PORT1_AREF — INPUT

| | | |
|---|---|---|
| 1 | TPB- | TPB(R) |
| 9 | | TPB<R> |
| 2 | TPB+ | TPB+ |
| 8 | VP | |
| 7 | VC/NC | |
| 6 | VG | |
| 3 | TPA- | TPA- |
| 5 | | TPA<R> |
| 4 | TPA+ | TPA(R) |
| 10 | | |
| 11 | CHASSIS GND | |
| 12 | | |
| 13 | | |

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

# Late-VG Protection Power

8 =PP3V3_FW_LATEVG — R4390 332 1% 1/16W MF-LF 402 — PP2V4_FW_LATEVG (37 38)
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V

CRITICAL
D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

## FireWire Ports

SYNC_MASTER=SENSOR — SYNC_DATE=08/14/2008


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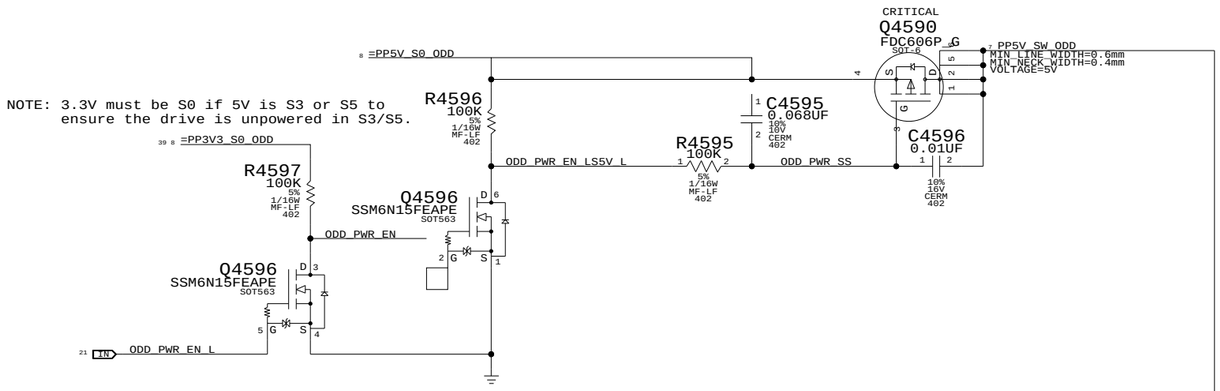
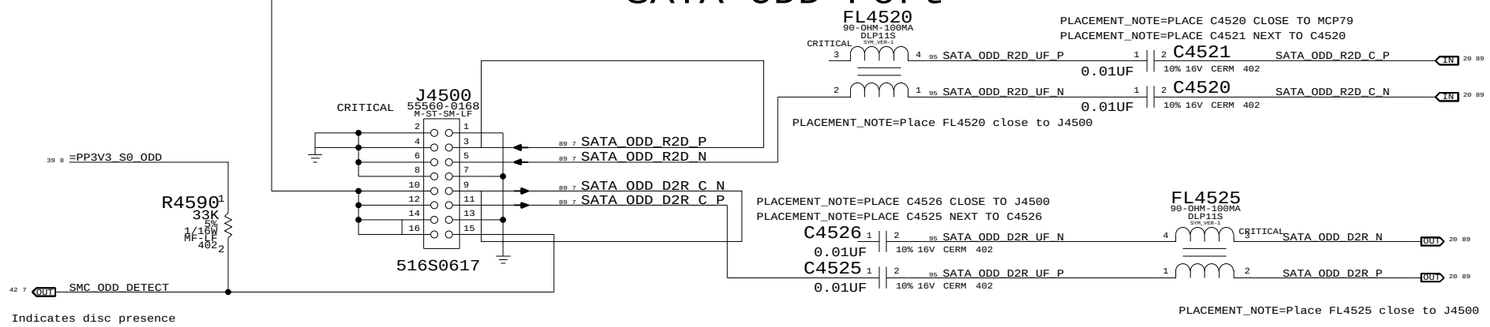
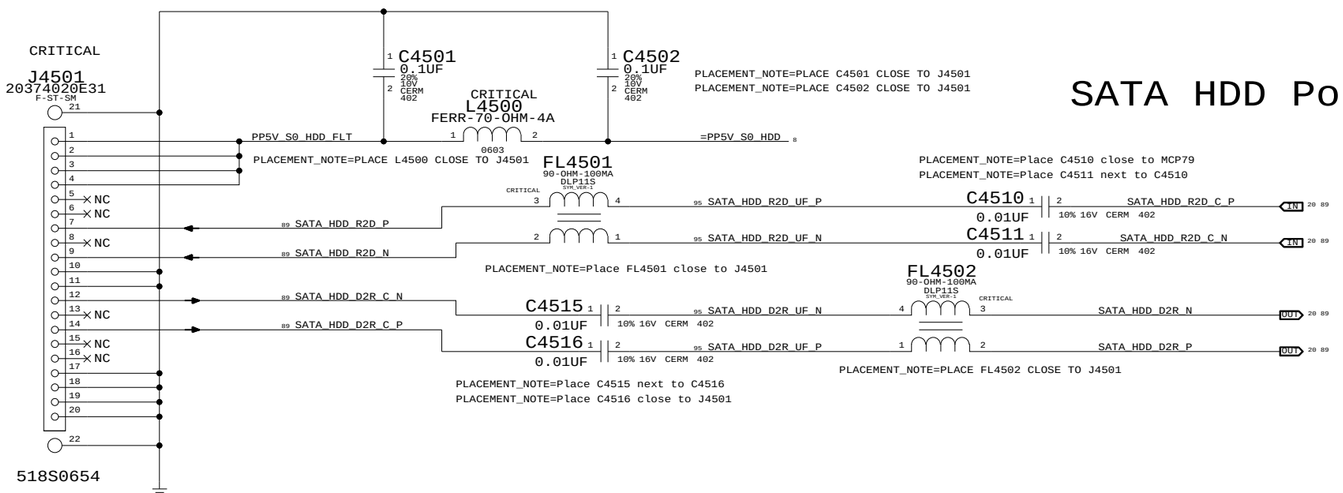
# ODD Power Control




# SATA ODD Port




# SATA HDD Port




# SATA Connectors

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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 45 OF 109 | |

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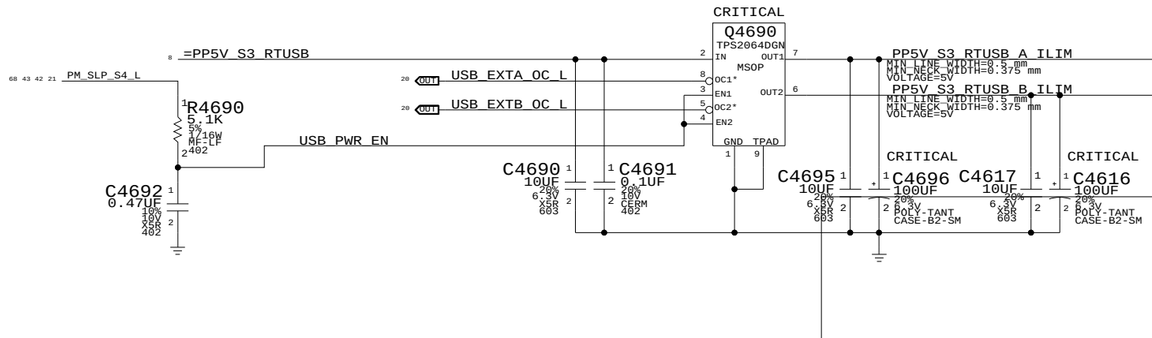
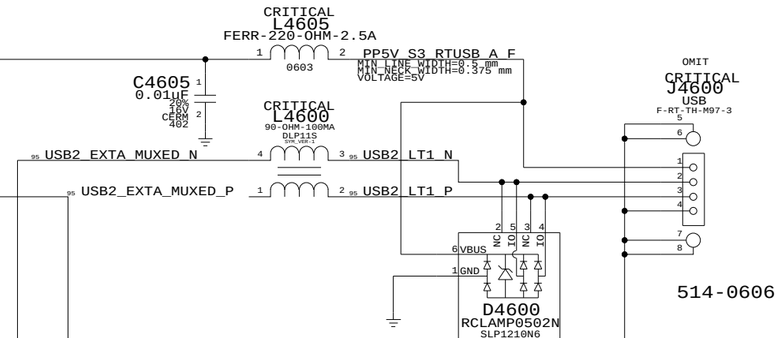
## Port Power Switch

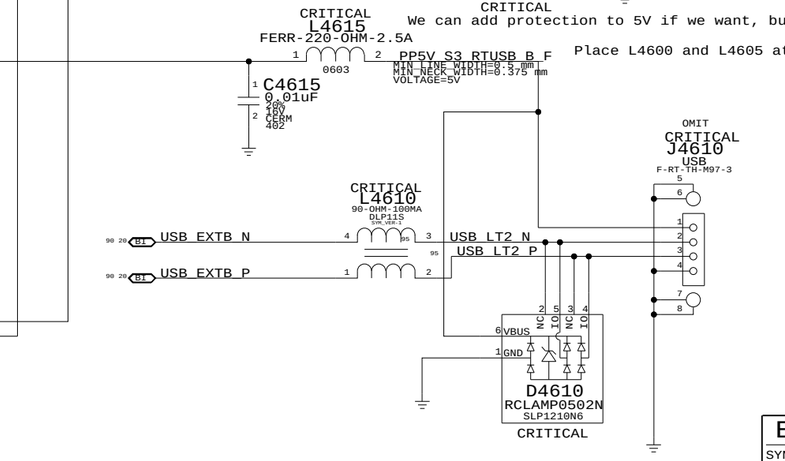



## Left USB Port A

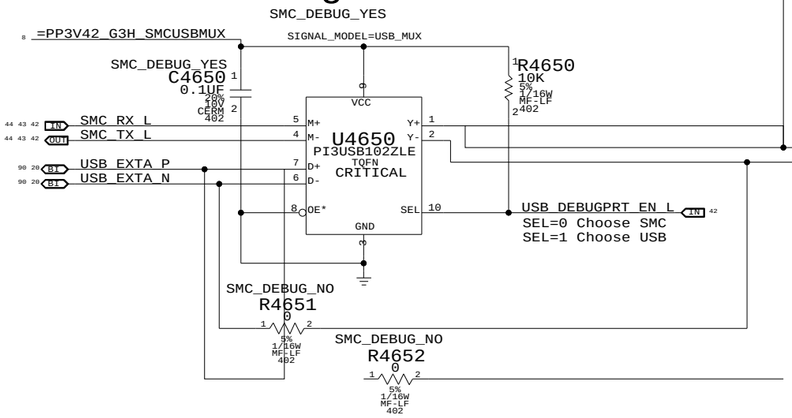



We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin




## USB/SMC Debug Mux




## Left USB Port B

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 514-0638 | 2 | CONN,RCPT,USB,HB,4P | J4600, J4610 | CRITICAL | |

# External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 46 OF 109 | |

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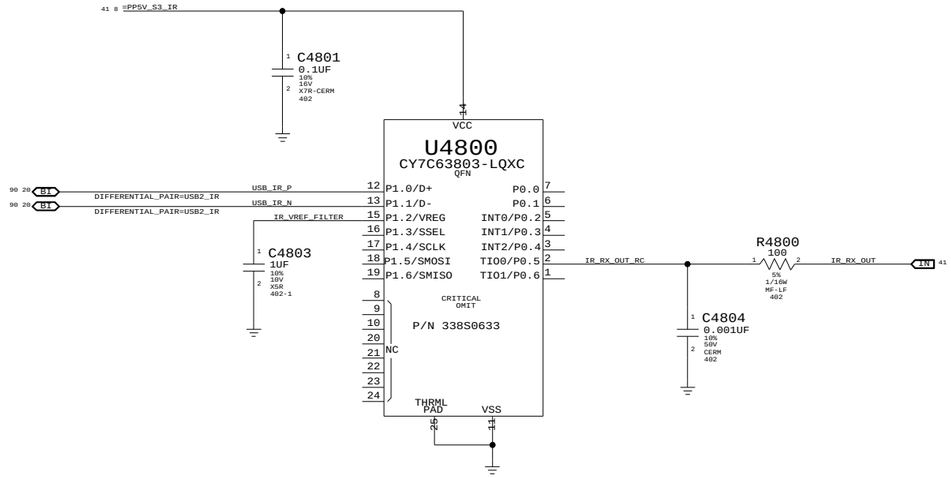


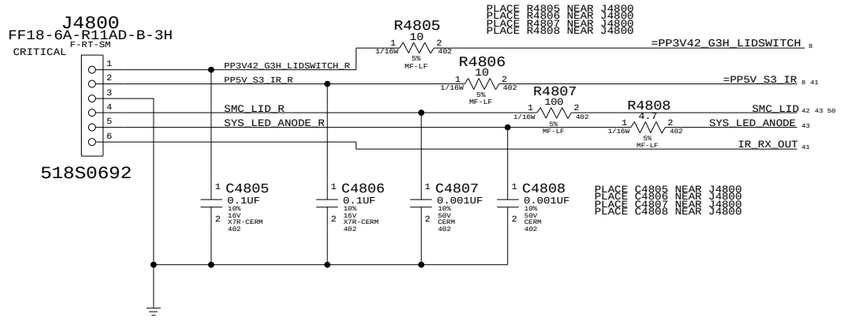


Front Flex Support

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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|---|---|---|
| D | 051-7902 | D |
| SCALE | SHT | OF |
| NONE | 48 | 109 |

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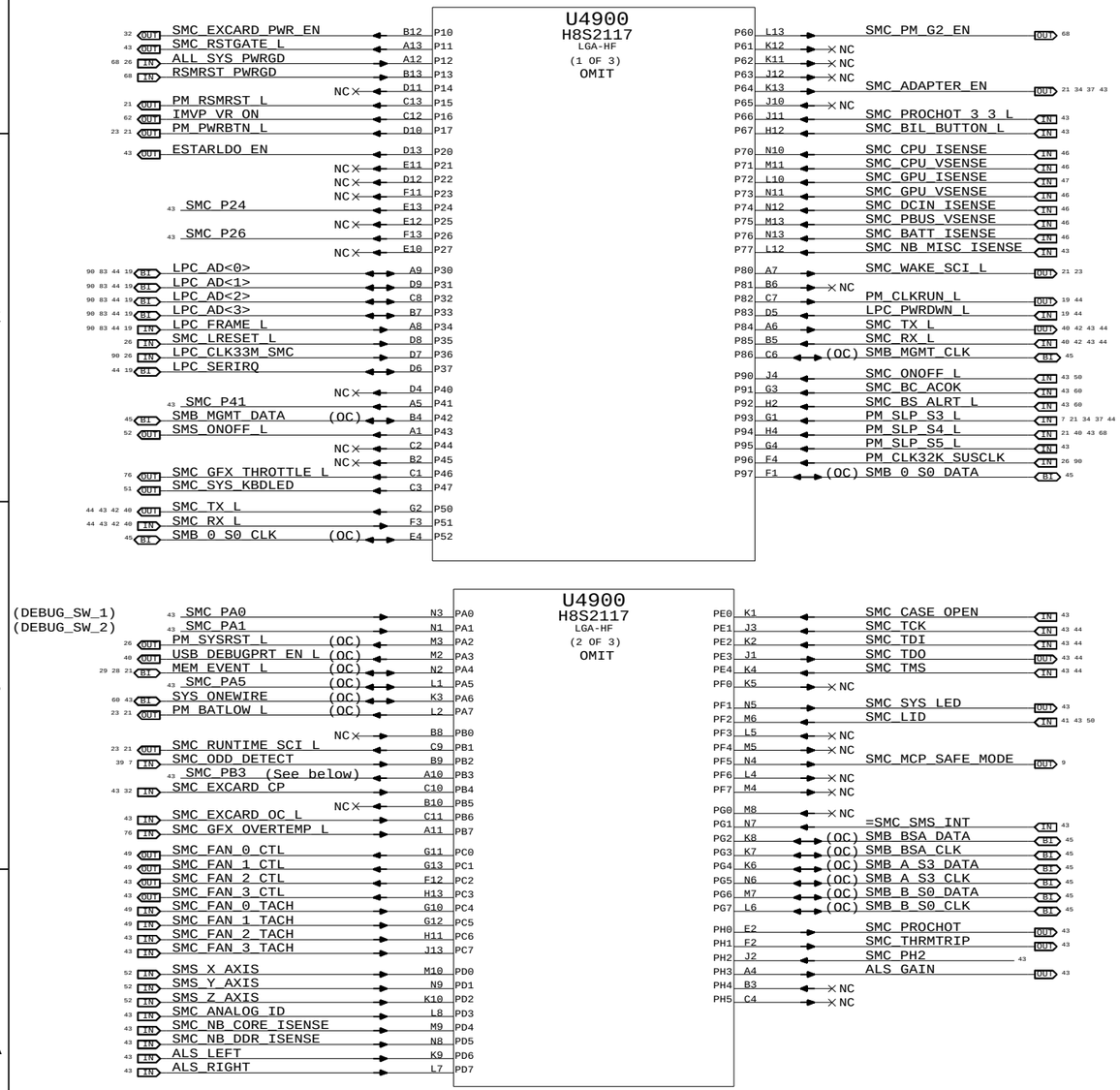
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

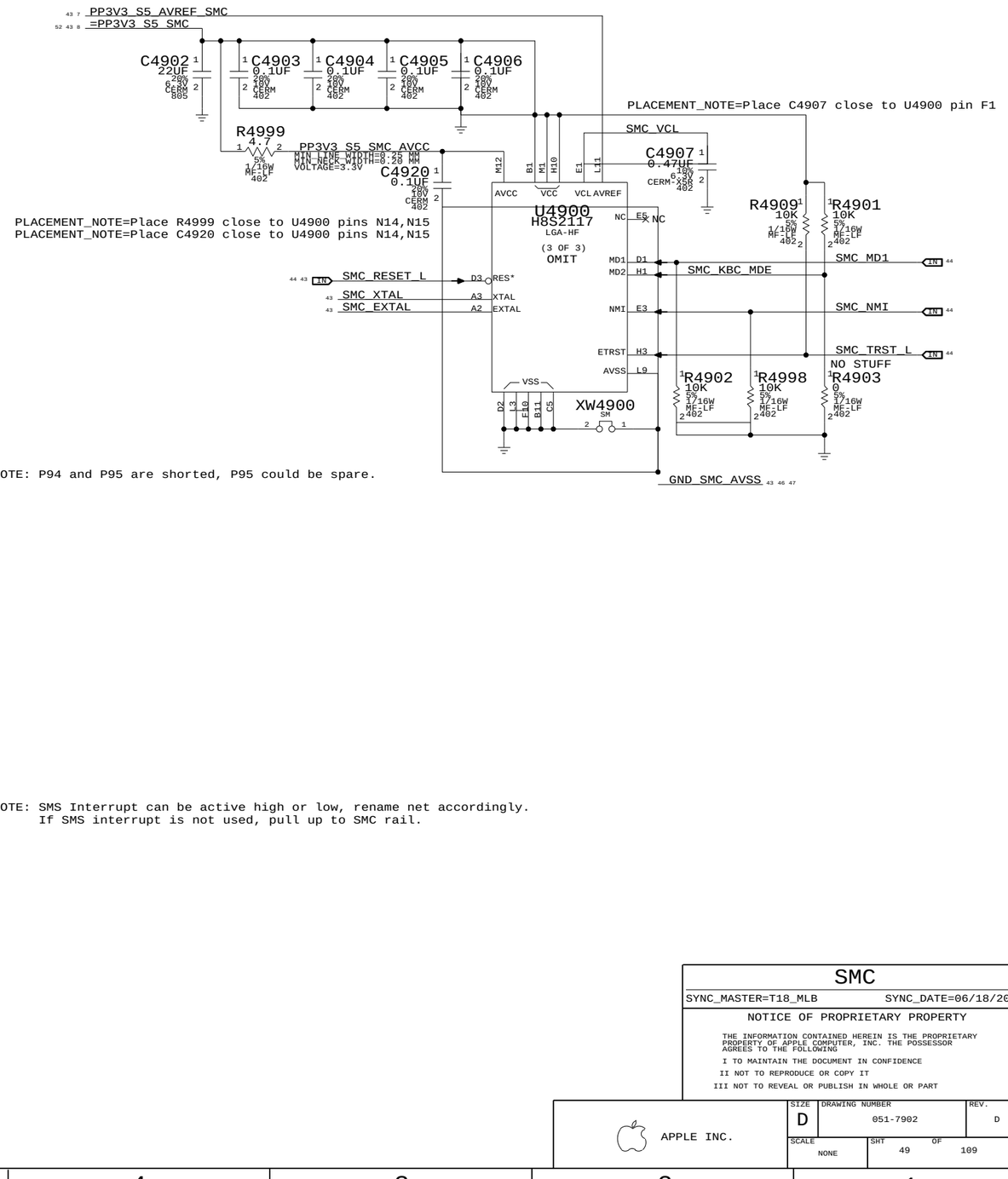






SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)




NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

| SMC | | |
|---|---|---|
| SYNC_MASTER=T18_MLB | | SYNC_DATE=06/18/2008 |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|---|---|---|---|
| | D | 051-7902 | D |
| | SCALE: NONE | SHT 49 OF 109 | |

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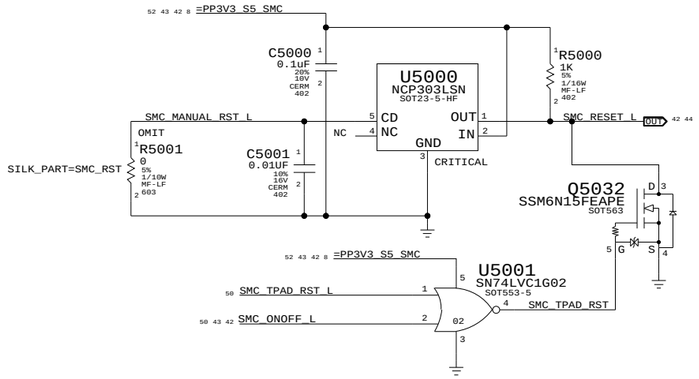
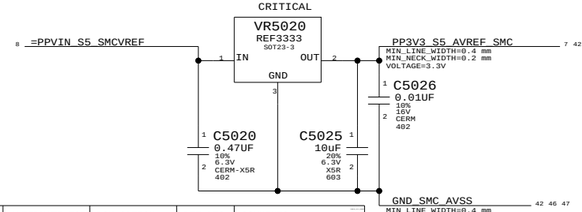
## SMC Reset "Button" / Brownout Detect

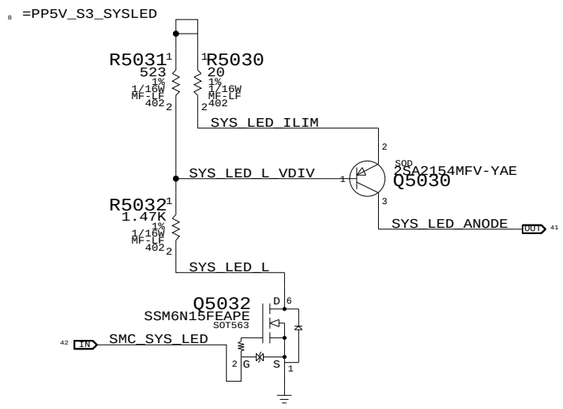



## SMC AVREF Supply

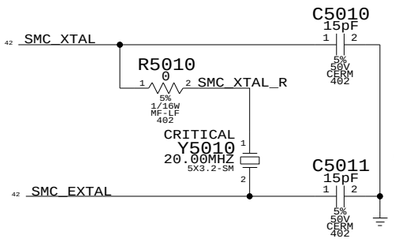



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 353S1381 | 353S1912 | | ALL | Intersil ISL60002-33 |

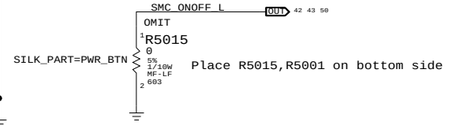
## System (Sleep) LED Circuit

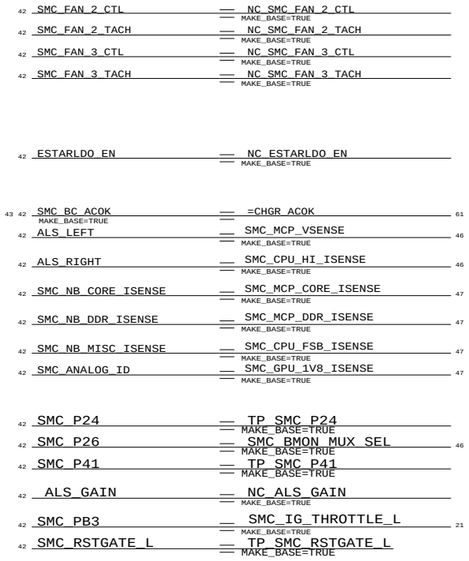



## SMC Crystal Circuit

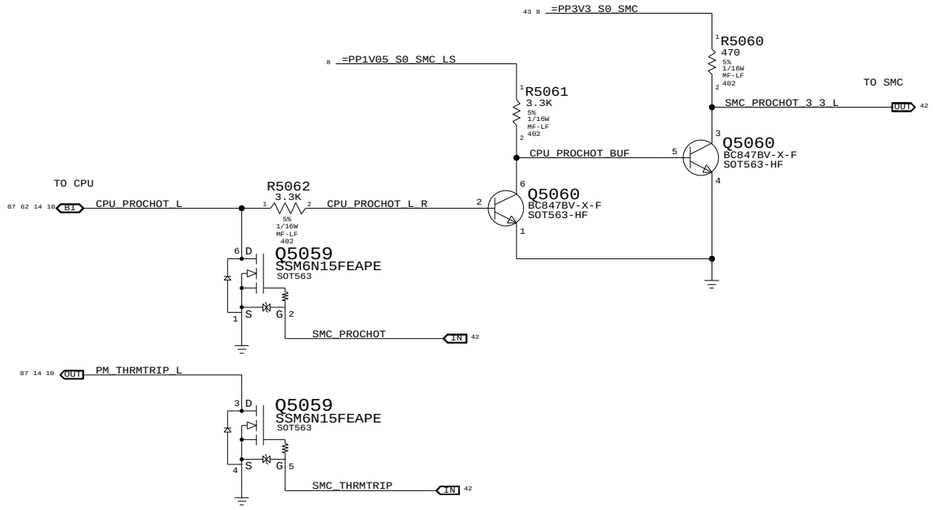



## Debug Power "Button"




## SMC FSB to 3.3V Level Shifting




## SMC Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

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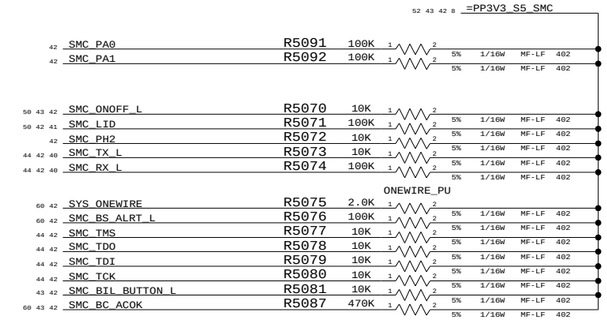
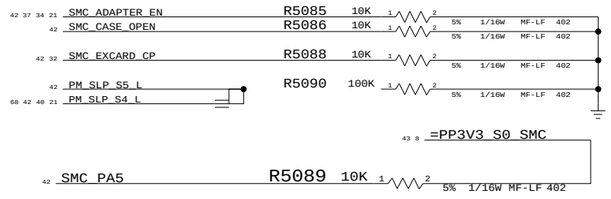
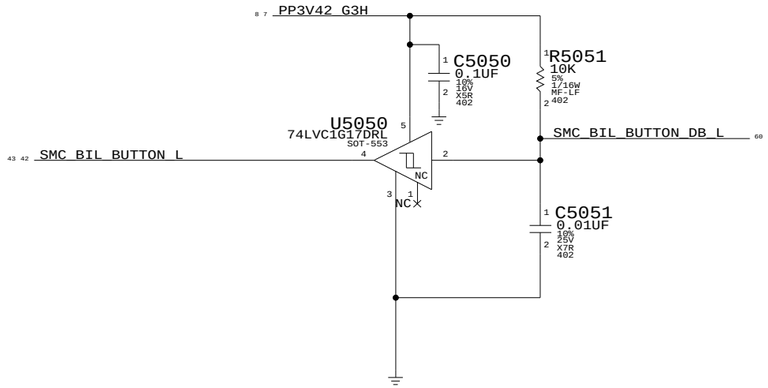
| SCALE | SHT | OF |
|---|---|---|
| NONE | 50 | 109 |


=PP3V3_S5_SMC
SMC_PA0 — R5091 100K 5% 1/16W MF-LF 402
SMC_PA1 — R5092 100K 5% 1/16W MF-LF 402
SMC_ONOFF_L — R5070 10K
SMC_LID — R5071 100K
SMC_PH2 — R5072 10K
SMC_TX_L — R5073 10K
SMC_RX_L — R5074 100K
ONEWIRE_PU
SYS_ONEWIRE — R5075 2.0K
SMC_BS_ALRT_L — R5076 100K
SMC_TMS — R5077 10K
SMC_TDO — R5078 10K
SMC_TDI — R5079 10K
SMC_TCK — R5080 10K
SMC_BIL_BUTTON_L — R5081 10K
SMC_BC_ACOK — R5087 470K

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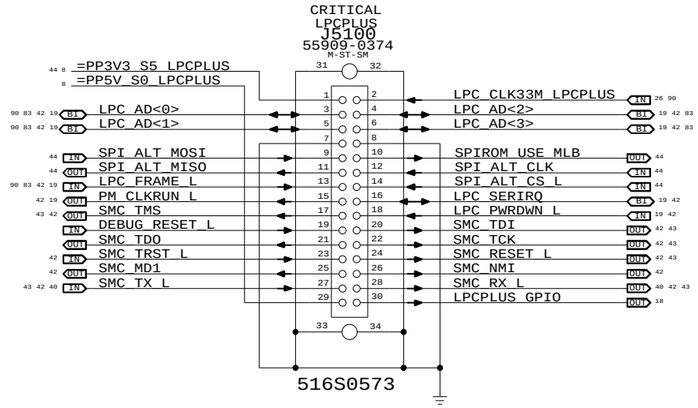
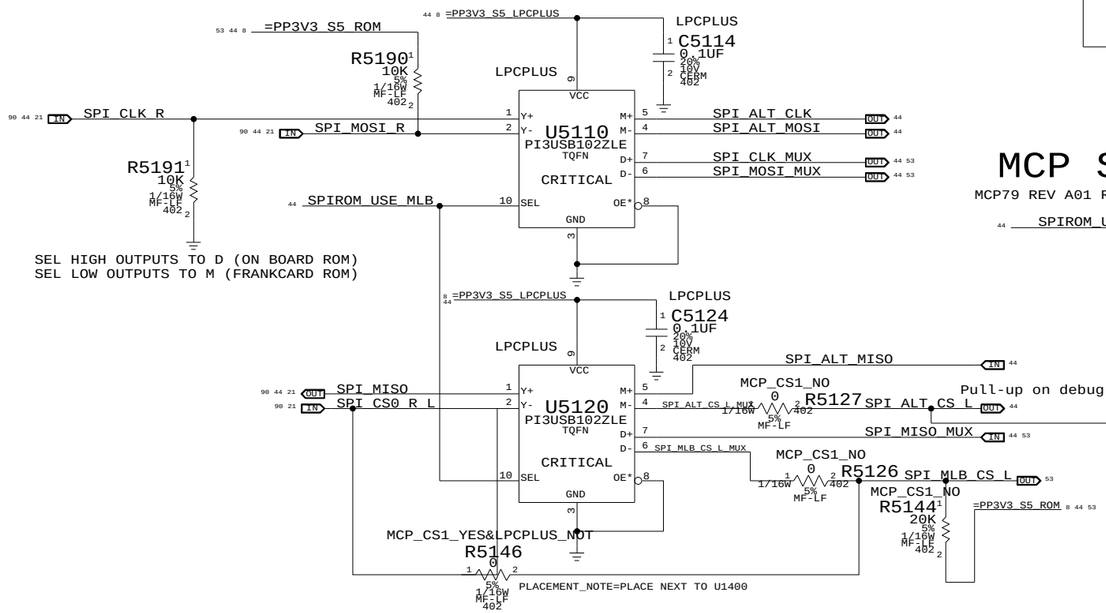
# LPC+SPI Connector



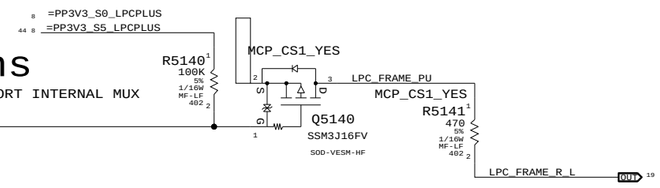

# Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP



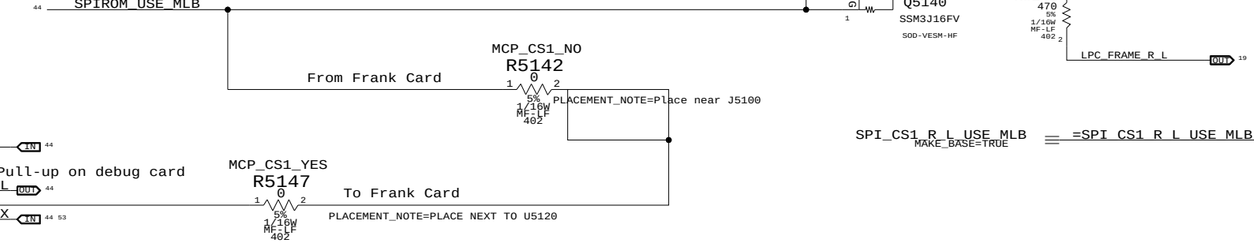

# MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON



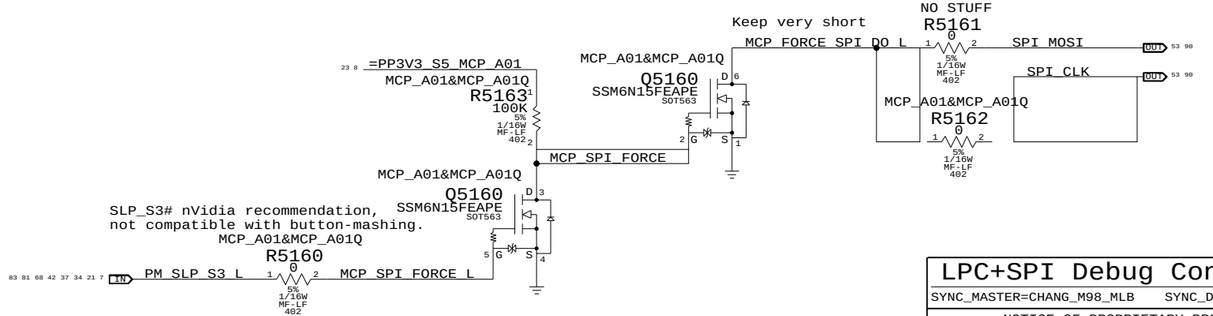

# MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

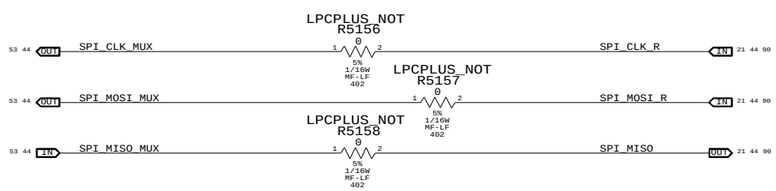



# SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED.NOT NEEDED FOR B01 OR LATER.




# SPI MUX BYPASS




# LPC+SPI Debug Connector

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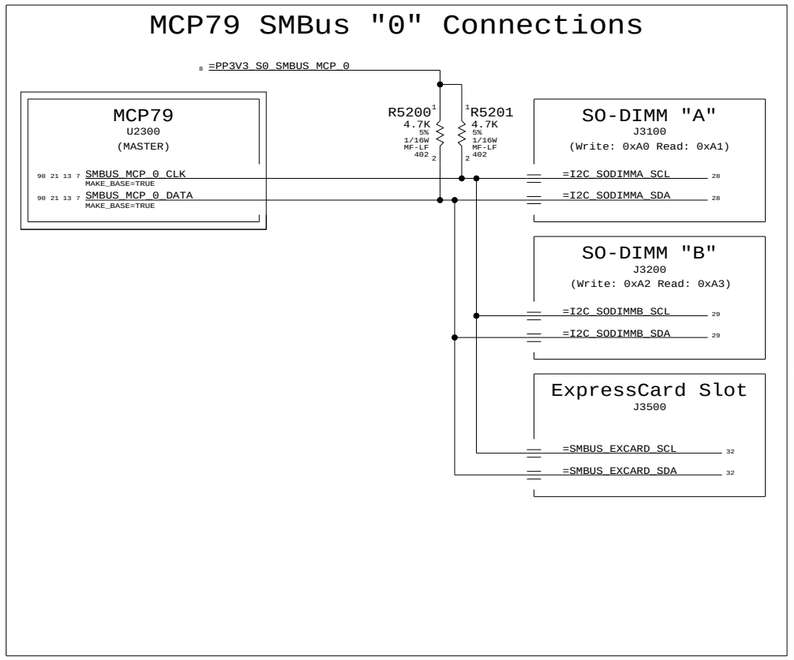


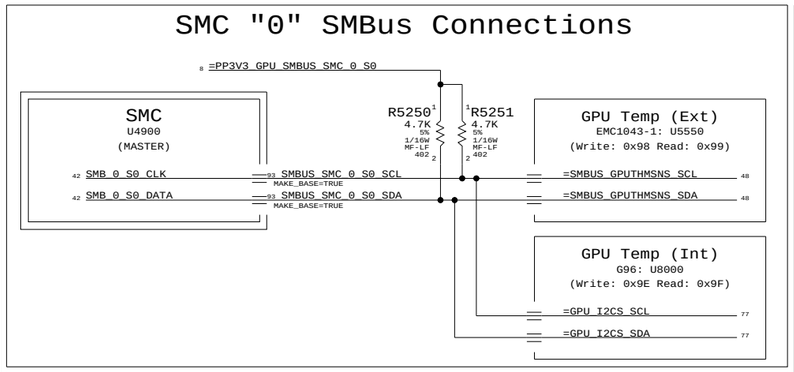


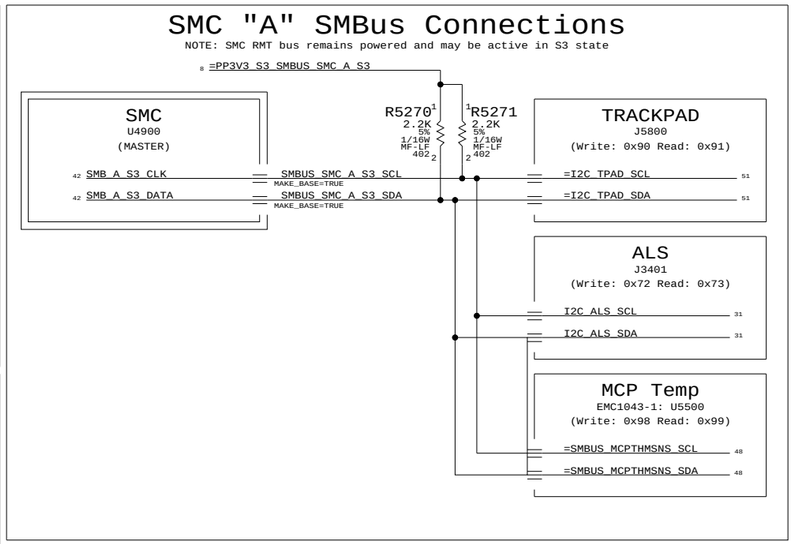


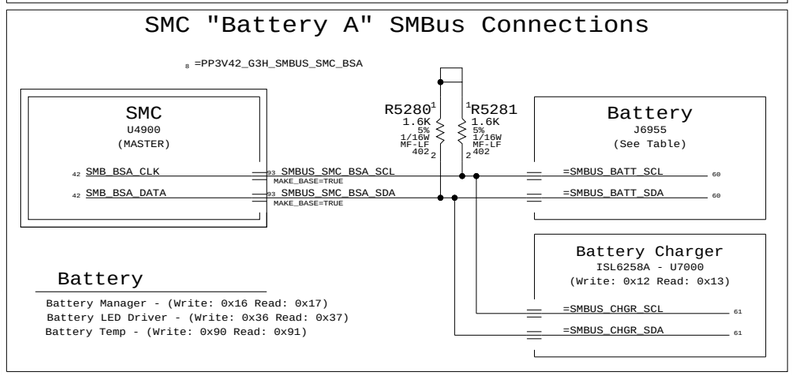


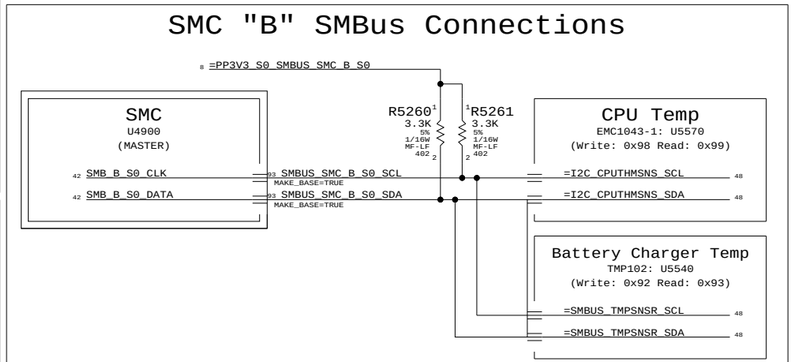


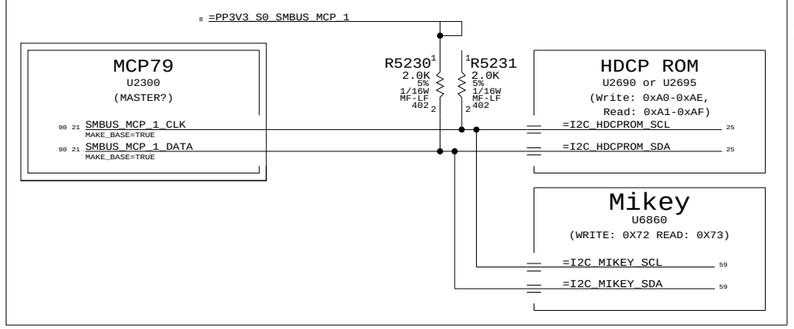


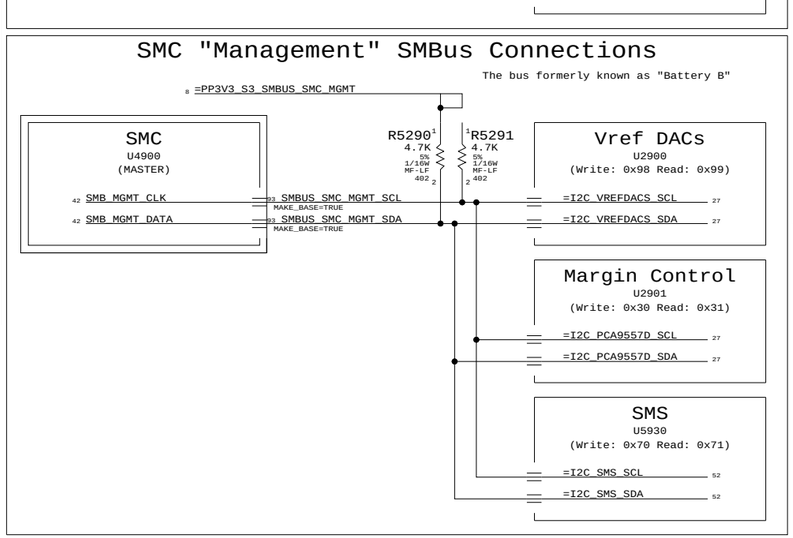


M98 SMBus Connections

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 52 OF 109 | |

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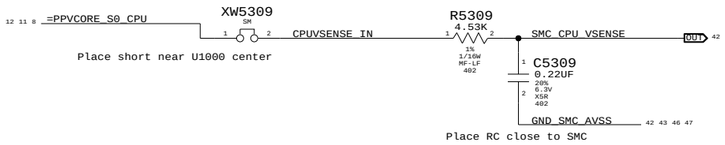
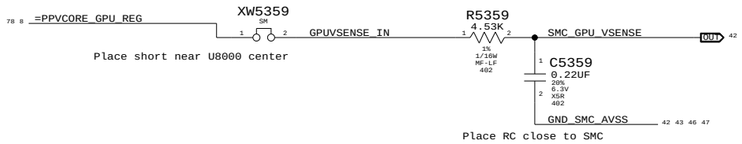
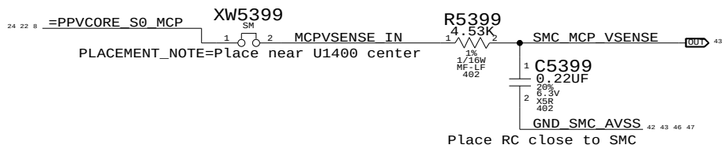
## CPU Voltage Sense / Filter



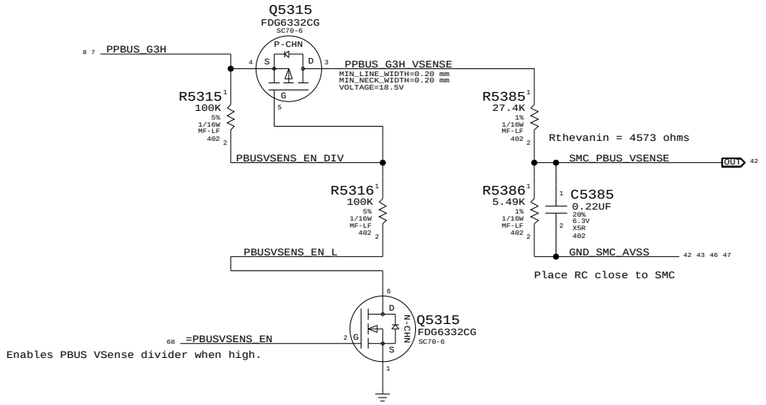

## GPU Voltage Sense / Filter



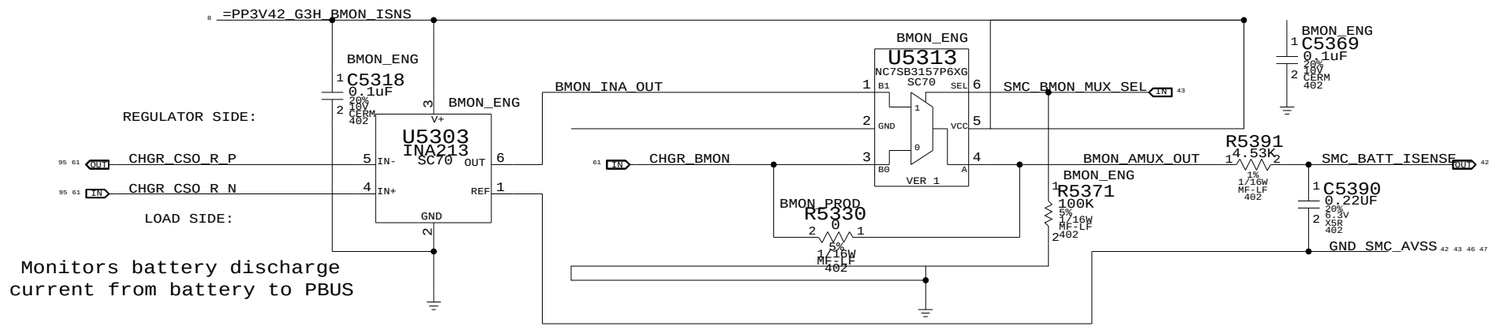

## MCP Voltage Sense / Filter



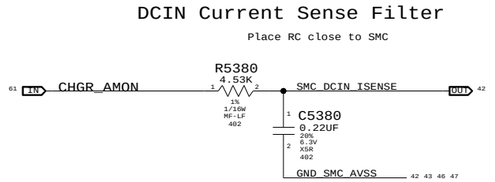

## PBUS Voltage Sense & Filter



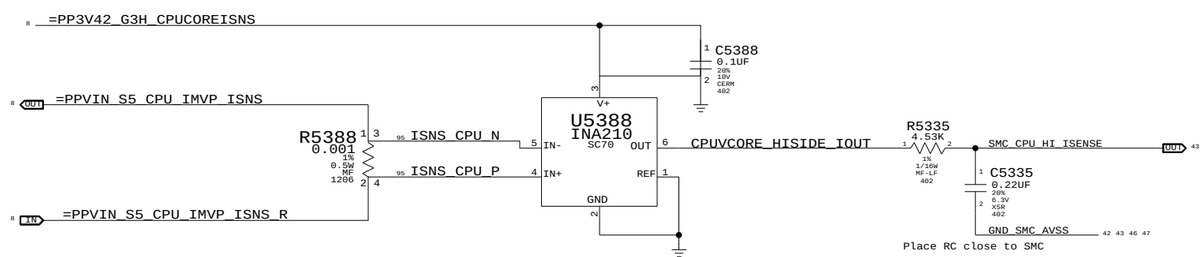

## BMON Current Sense - Entire circuit must be near SMC (U4900)



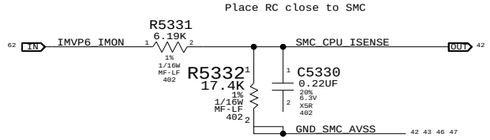

## DCIN Current Sense Filter




## CPU VCore High Side Current Sensor




## CPU VCore Load Side Current Sense / Filter





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# Current & Voltage Sensing

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|---|---|---|
| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 53 | 109 |

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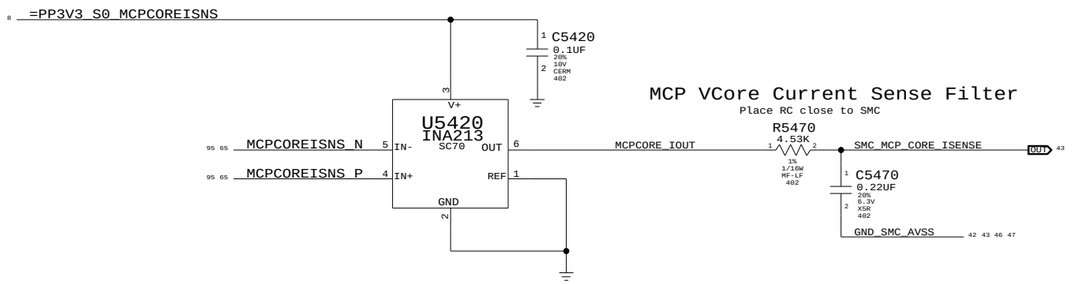
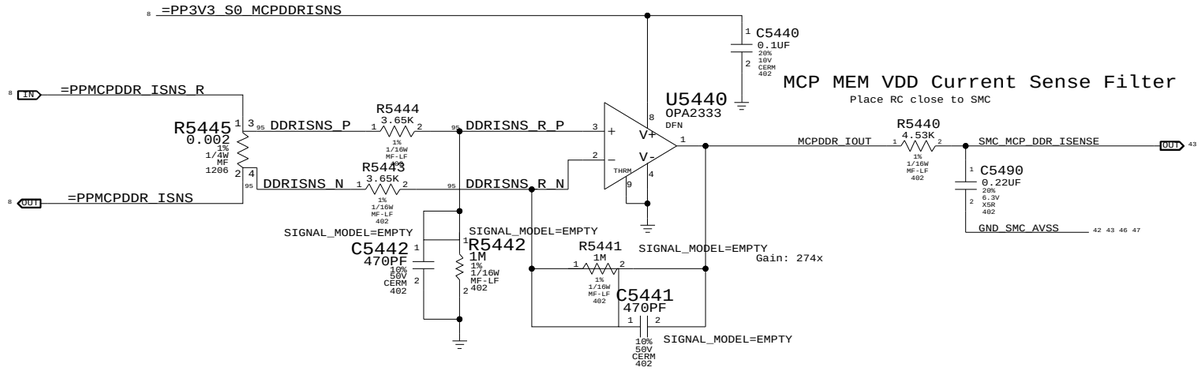
## MCP VCore Current Sense




### MCP VCore Current Sense Filter

Place RC close to SMC

## MCP MEM VDD Current Sense



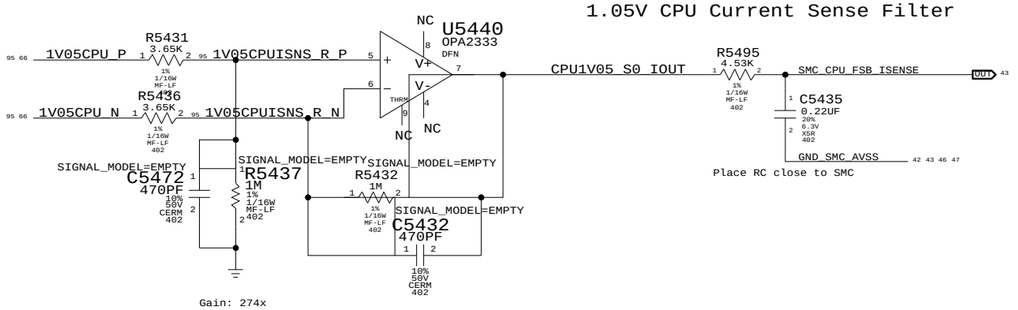

### MCP MEM VDD Current Sense Filter

Place RC close to SMC

OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

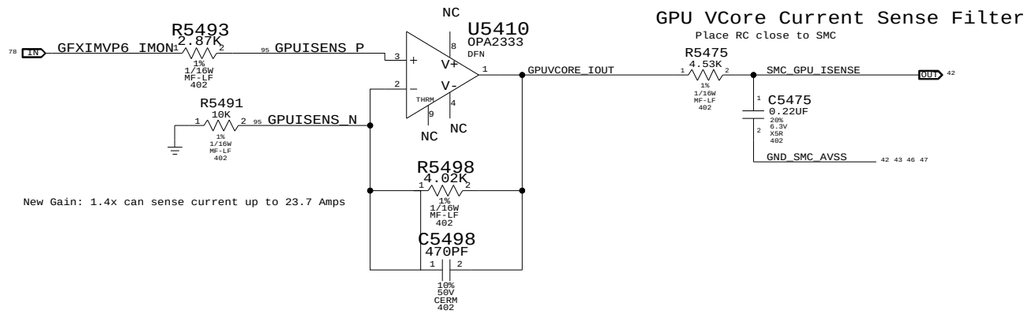
## CPU FSB 1.05V Current Sense




### 1.05V CPU Current Sense Filter

Place RC close to SMC

## GPU VCore Current Sense



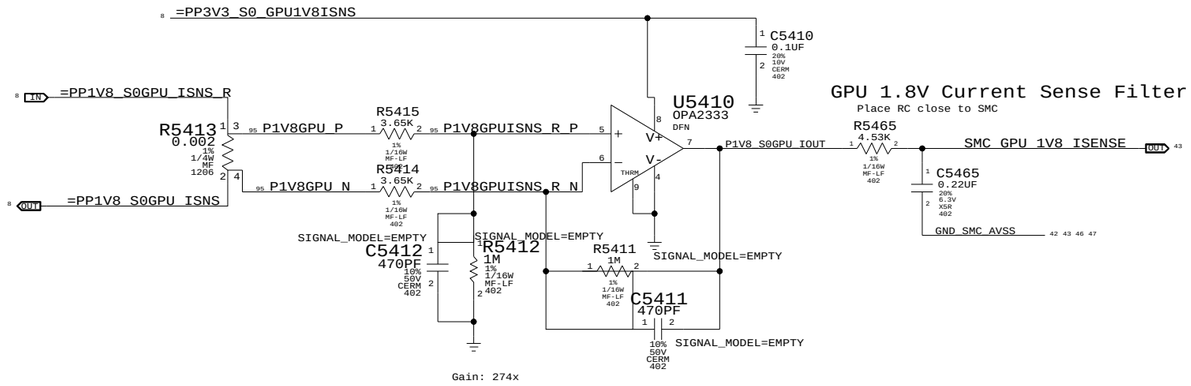

### GPU VCore Current Sense Filter

Place RC close to SMC

New Gain: 1.4x can sense current up to 23.7 Amps

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

## GPU 1.8V Current Sense




### GPU 1.8V Current Sense Filter

Place RC close to SMC

| Current Sensing | |
|---|---|
| SYNC_MASTER=SENSOR | SYNC_DATE=08/14/2008 |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|---|---|---|---|
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| | SCALE: NONE | SHT 54 OF 109 | |

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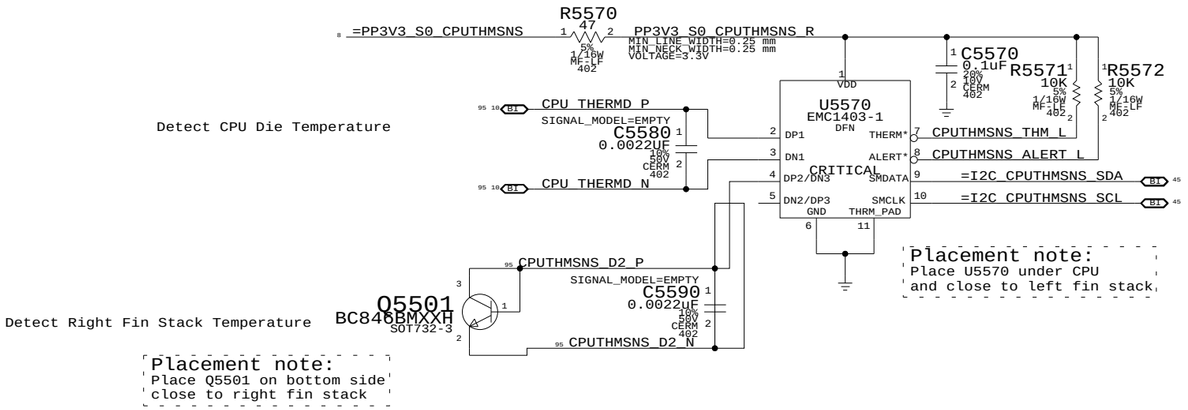
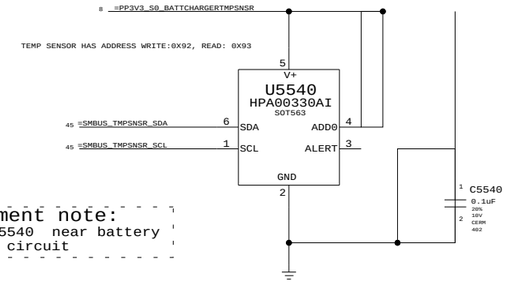
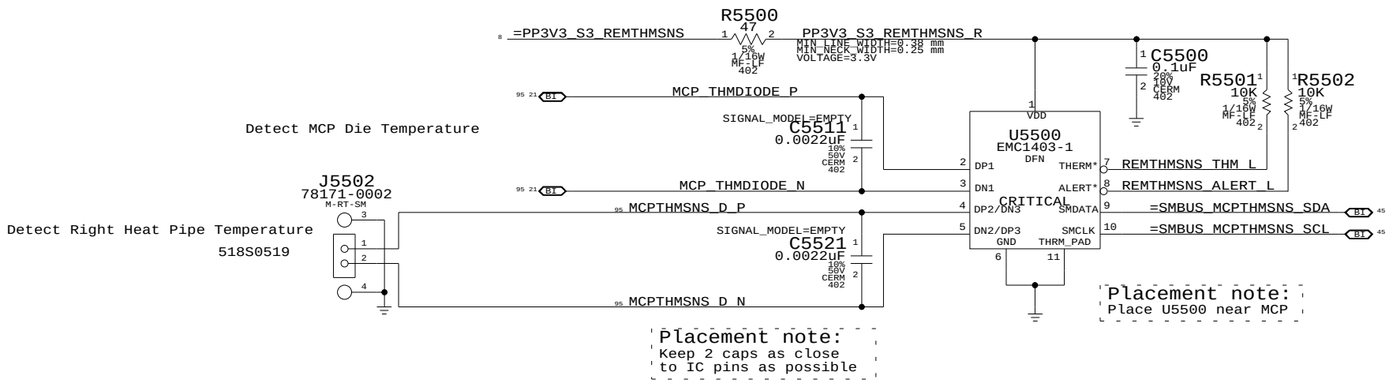
# CPU Proximity/CPU Die/Right Fin Stack




# Battery Charger Proximity

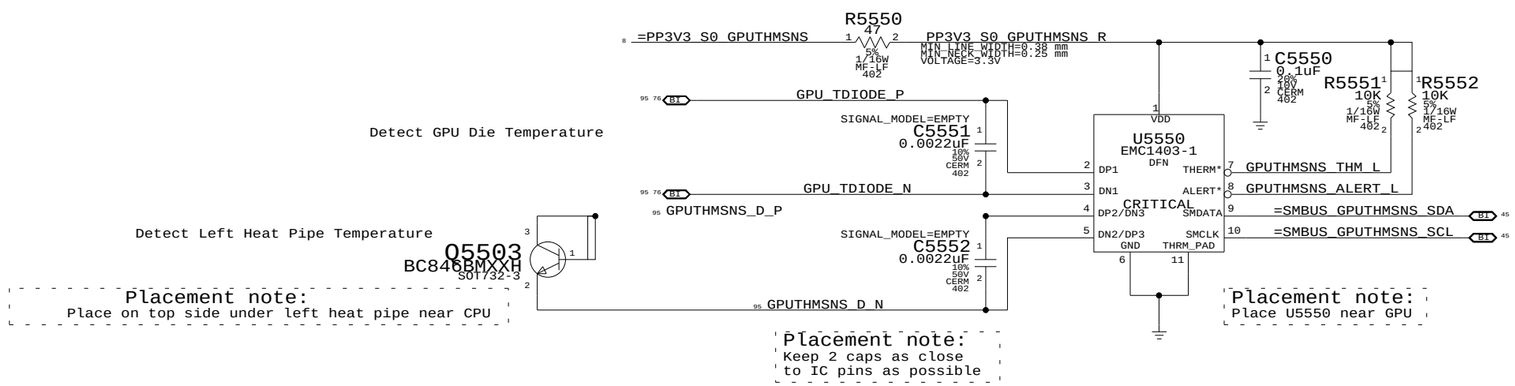



# MCP Proximity/MCP Die/Right Heat Pipe




Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

# GPU Proximity/GPU Die/Left Heat Pipe




## Thermal Sensors

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008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| SCALE: NONE | SHT 55 OF 109 | |

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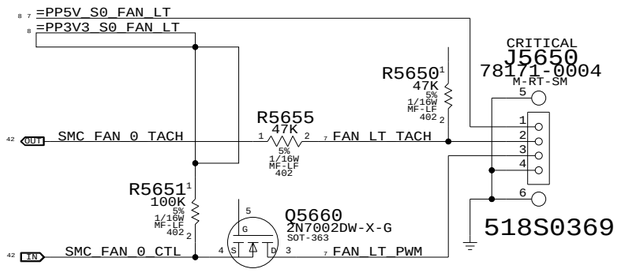
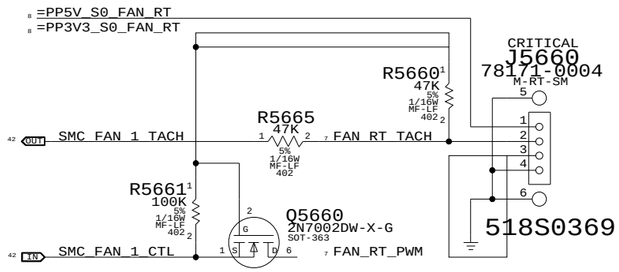
## Left Fan




## Right Fan




# Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007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| SCALE | SHT | OF |
|---|---|---|
| NONE | 56 | 109 |

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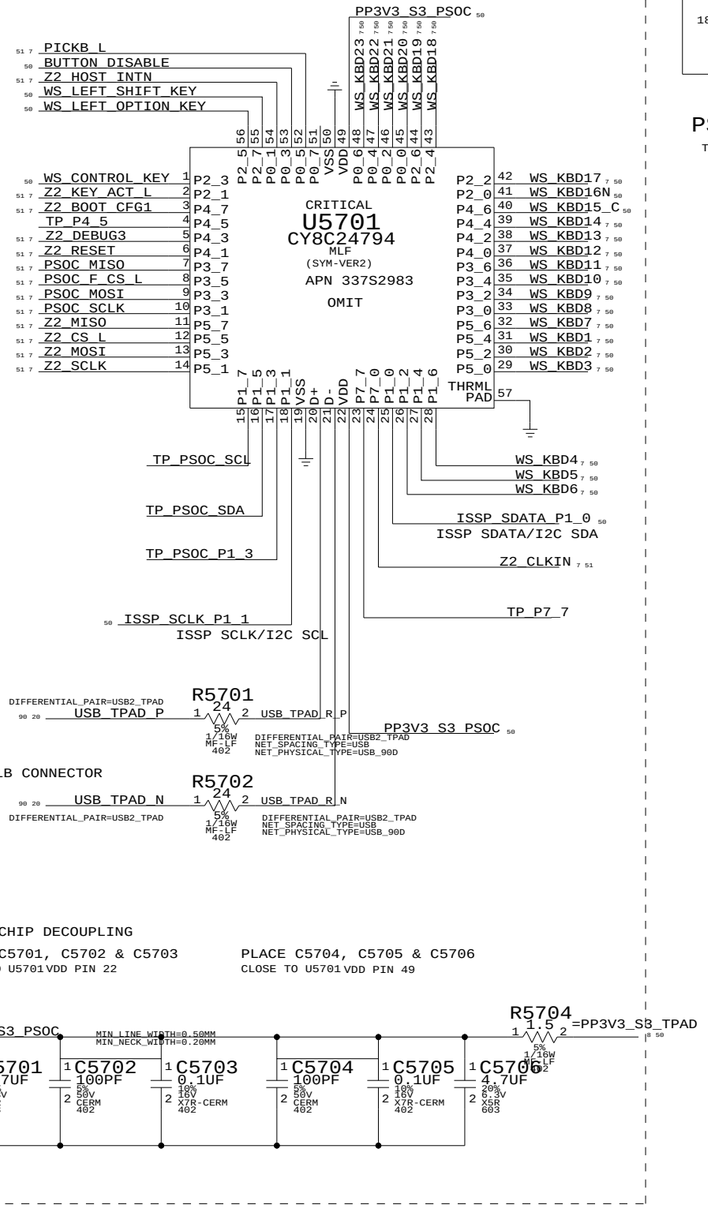
# PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

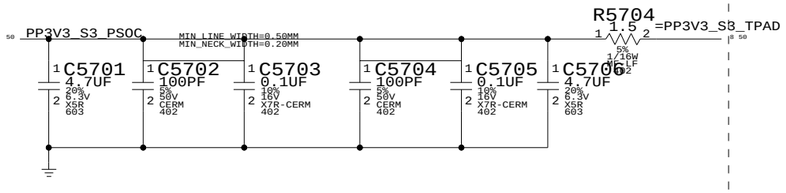
TRACKPAD PICK BUTTONS
KEYBOARD SCANNER




U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

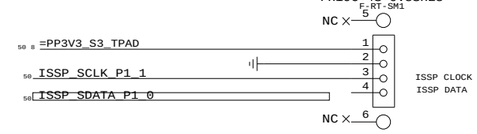



| IC | PIN NAME | CURRENT | R_SNS | V_SNS | POWER |
|---|---|---|---|---|---|
| TMP102 | V+ | 10UA<br>80UA | 2.55 KOHM | 0.0255 V<br>0.204 V | 0.255E-6 W<br>16.32E-6 W |
| 3V3 LDO | VDD | 60MA MAX | 10 OHM | 0.6 V | 36E-3 W |
| | VOUT | 60MA MAX | 0.2 OHM | 0.012 V | 0.72E-3 W |
| PSOC | VDD | 8MA (TYP)<br>14MA (MAX) | 1.5 OHM | 0.012 V<br>0.021 V | 96E-6 W<br>294E-6 W |
| 18V BOOSTER | VIN | 4MA (MAX) | 4.7 OHM | 0.0188 V | 75.2E-6 W |

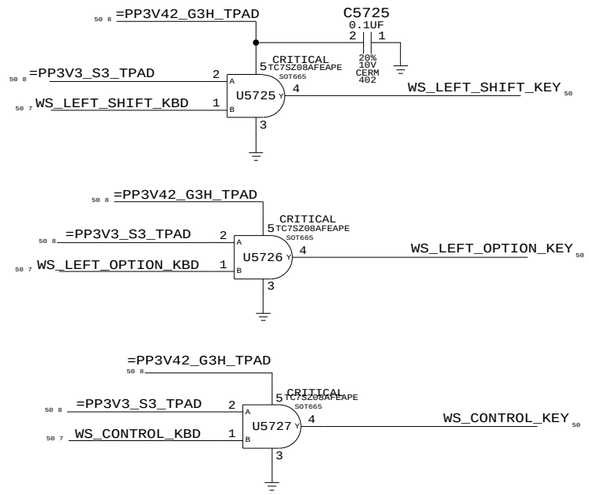
## PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

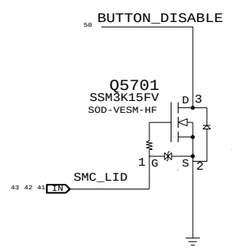
TPAD_DEBUG
APN 518S0430




## ISOLATION CIRCUIT




## TPAD BUTTONS DISABLE

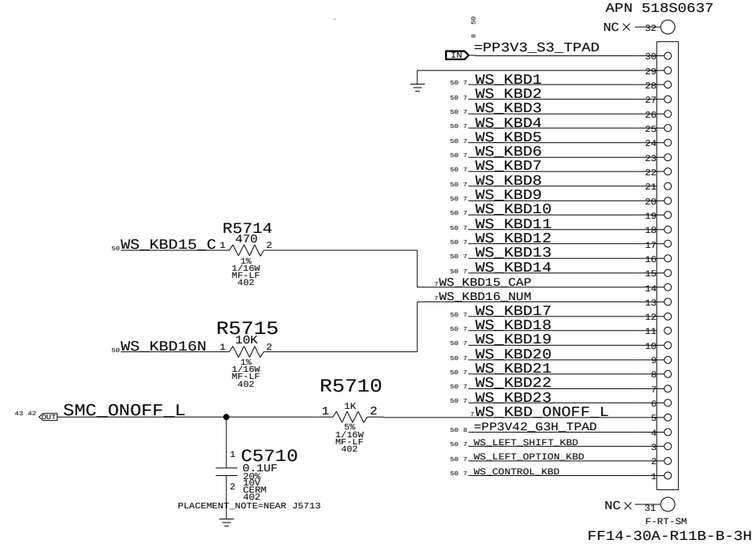



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

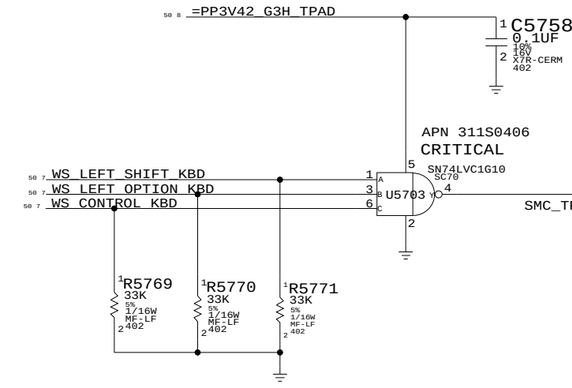
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

## KEYBOARD CONNECTOR

J5713
APN 518S0637




## SMC_MANUAL_RESET LOGIC





WELLSPRING 1
SYNC_MASTER=AMASON_M99 SYNC_DATE=06/18/2008

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# BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

PLACEMENT_NOTE=under L5800 on top side
R5800 0 5% 1/10W MF-LF 603
NO STUFF
CRITICAL
PLACEMENT_NOTE=NEAR J5800
=PP5V_S3_TPAD
L5800 0.01H-0.3A-80V SM-HF SYM_VER=1
VOLTAGE=3V3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
C5800 0.1UF 20% 10V CERM 402
PP5V_S3_TPAD_F
TPAD_GND_F
PLACEMENT_NOTE=NEAR J5800
VOLTAGE=0V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
R5801 0 5% 1/10W MF-LF 603
PLACEMENT_NOTE=under L5800 on top side

PP5V_S3_TPAD_F
R5805 0 5% 1/4W MF-LF 402
APN 152S0504
CRITICAL
L5801 3.3UH-870MA
INPUT_SW
VLF3010AT-SM-HF
BOOST_SW
D5802 SOD-323
B0520WSXG
APN 371S0318
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
SWITCH_NODE=TRUE
PP18V5_S3_SW
R5806 0 5% 1/16W MF-LF 402
PP18V5_S3
PP5V_S3_BOOSTER
APN 353S1401
C5818 39PF 5% 50V CERM 402
R5812 1M 1% 1/16W MF-LF 402
C5819 1UF 10% 25V X5R 603-1
U5805 TPS61045 QFN
VIN
FB
CTRL
SW
PGND
GND
THRML PAD
BOOST_FB
Z2_BOOST_EN
R5813 71.5K 1% 1/16W MF-LF 402
C5816 0.1UF 10% 16V X7R-CERM 402
C5817 2.2UF 10% 16V X5R 603
R5811 100K 1% 1/16W MF-LF 402
TPAD_GND_F

3V3 LDO FOR IPD

R5873 10 1% 1/10W MF-LF 402
PP5V_S3_TPAD_F
PP5V_S3_VR
CRITICAL
APN 353S1364
C5853 2.2UF 10% 16V X5R 603
VR5802 MM3243DRRE NLF
VDD
CE
VOUT
GND
PP3V3_S3_LDO_R
R5836 0 5% 1/16W MF-LF 402-HF
PP3V3_S3_LDO
C5838 0.1UF 10% 16V X7R-CERM 402
C5854 4.7UF 20% 6.3V X5R 603
TPAD_GND_F

# IPD FLEX CONNECTOR

APN 516S0689
CRITICAL
J5800 55560-0228 M-ST-SM

| | | | |
|---|---|---|---|
| TPAD_GND_F | 2 | 1 | |
| Z2_CS_L | 4 | 3 | Z2_KEY_ACT_L |
| Z2_DEBUG3 | 6 | 5 | Z2_RESET |
| Z2_MOSI | 8 | 7 | PSOC_F_CS_L |
| Z2_MISO | 10 | 9 | PICKB_L |
| Z2_SCLK | 12 | 11 | PSOC_MISO |
| Z2_BOOST_EN | 14 | 13 | PSOC_MOSI |
| Z2_HOST_INTN | 16 | 15 | PSOC_SCLK |
| Z2_BOOT_CFG1 | 18 | 17 | =I2C_TPAD_SDA |
| Z2_CLKIN | 20 | 19 | =I2C_TPAD_SCL |
| PP3V3_S3_LDO | 22 | 21 | PP18V5_S3 |

# Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

=PP3V3_S0_TPAD
R5853 470K 5% 1/10W MF-LF 402
SMC_SYS_KBDLED
R5854 4.7K 5% 1/10W MF-LF 402
SMC_KDBLED_PRESENT_L
=PP5V_S0_KBDLED
CRITICAL
L5850 10UH-0.58A-0.35OHM 1098AS-SM
KBDLED_SW
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.25 MM
SWITCH_NODE=TRUE
C5850 1UF 10% 10V X5R 402-1
VIN
SW
CRITICAL
U5850 LT3491 DFN
CTRL
LED
CAP
GND
THRML PAD
NO STUFF
R5852 10K 5% 1/10W MF-LF 402
R5855 10 1% 1/16W MF-LF 402
KBDLED_CAP
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
C5855 1UF 10% 10V X5R 603
KBDLED_ANODE
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM

CRITICAL
J5815 FF18-4A-R11AD-B-3H F-RT-SM
J5815 pin 1 is grounded on keyboard backlight flex
SMC_KDBLED_PRESENT_L
APN 518S0612

KBD BACKLIGHT CONNECTOR

WELLSPRING 2
SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

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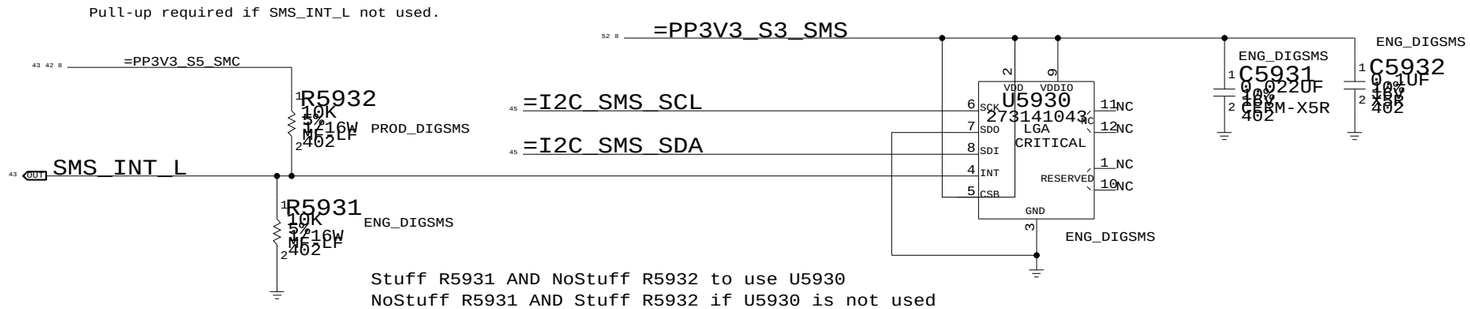
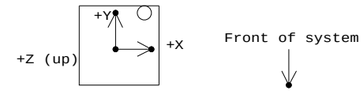
# Digital SMS



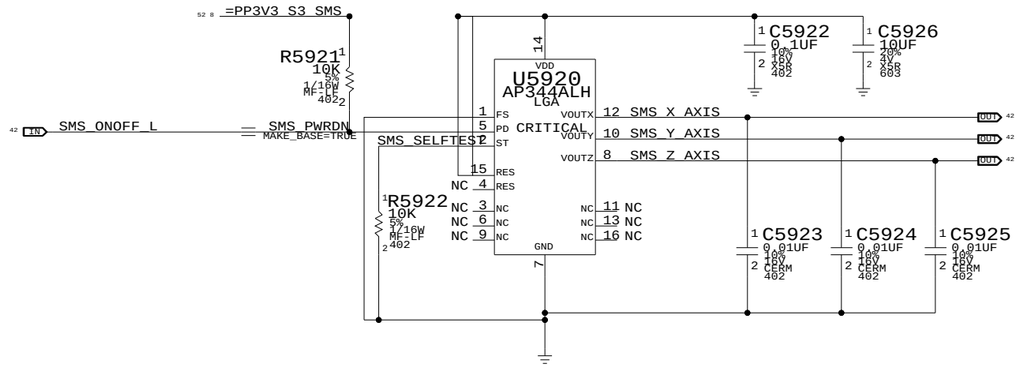

Desired orientation when
placed on board top-side:



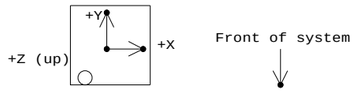

Circle indicates pin 1 location when placed
in correct orientation

# Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC




Desired orientation when
placed on board top-side:




Circle indicates pin 1 location when placed
in correct orientation

## Sudden Motion Sensor (SMS)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008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| SCALE: NONE | SHT 59 OF 109 | |

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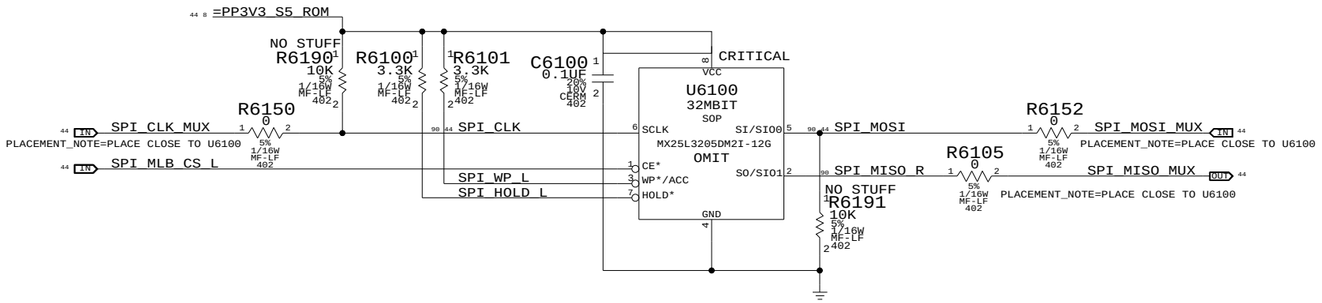


MCP79 SPI Frequency Select

| Frequency | SPI_MOSI | SPI_CLK |
|---|---|---|
| 31 MHz | 0 | 0 |
| 42 MHz | 0 | 1 |
| 25 MHz | 1 | 0 |
| 1 MHz | 1 | 1 |

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

# SPI ROM

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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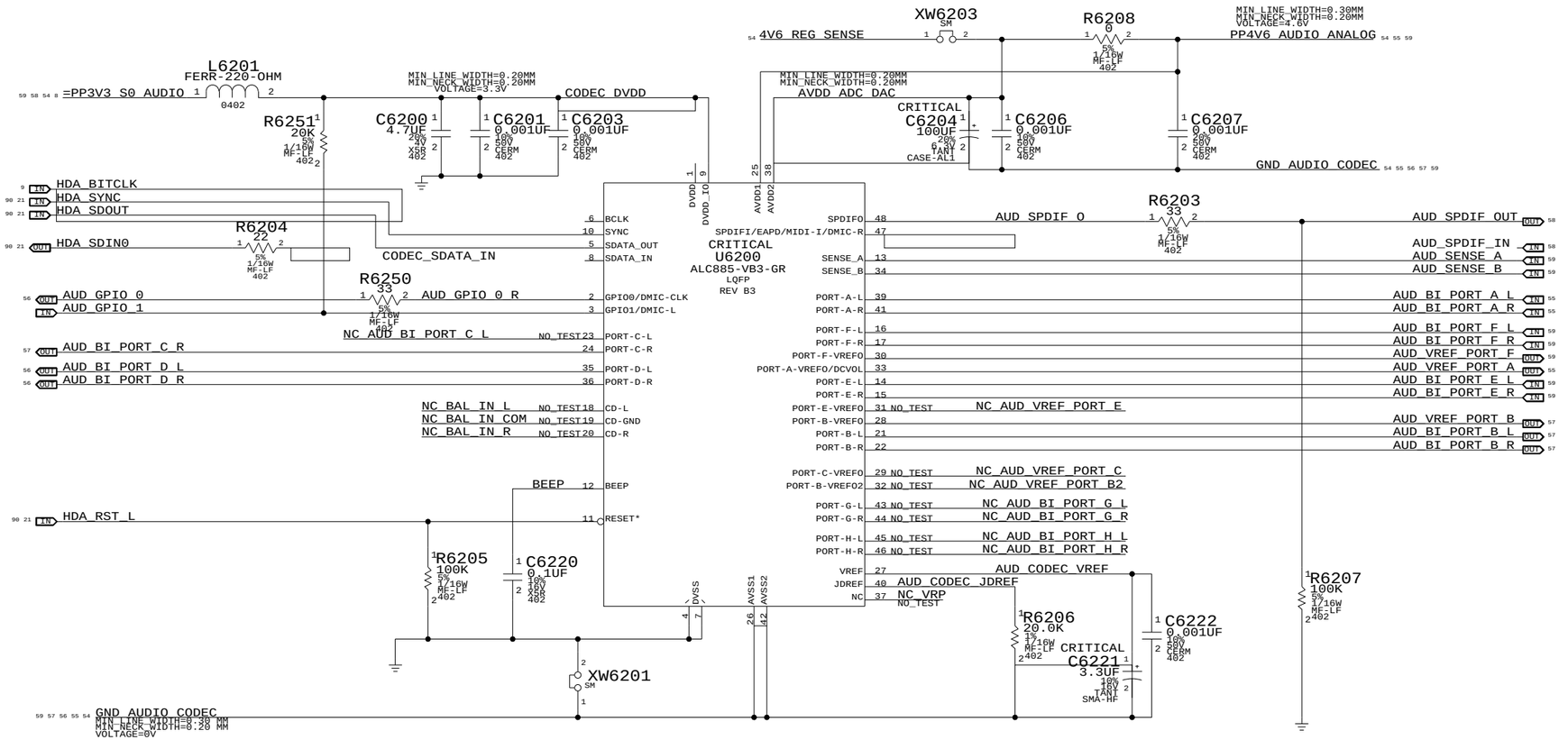
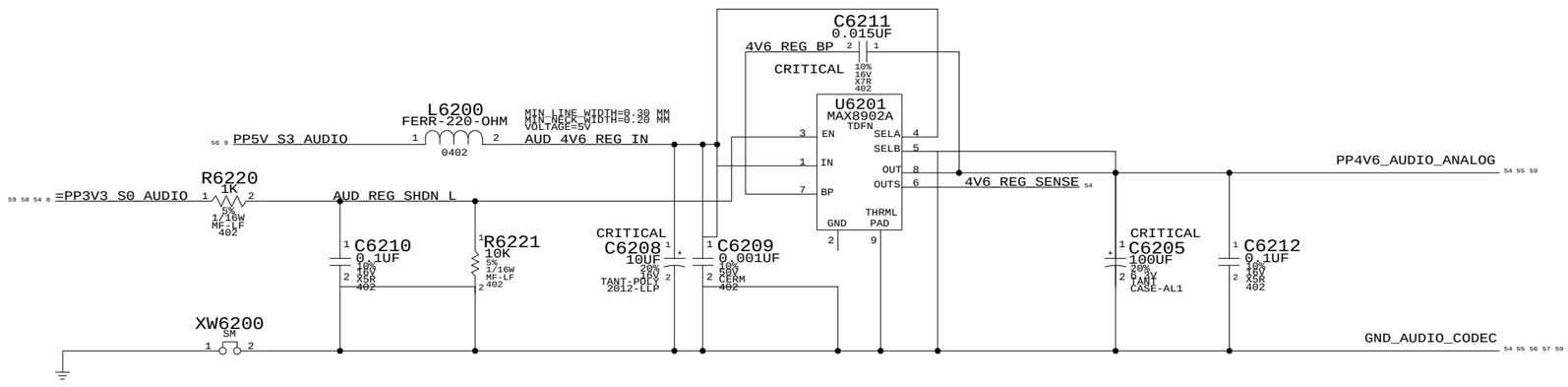
# AUDIO CODEC

APPLE P/N 353S1527




# AUDIO 4.6V REGULATOR

APPLE P/N 353S1897




## AUDIO:CODEC

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 62 OF 109 | |

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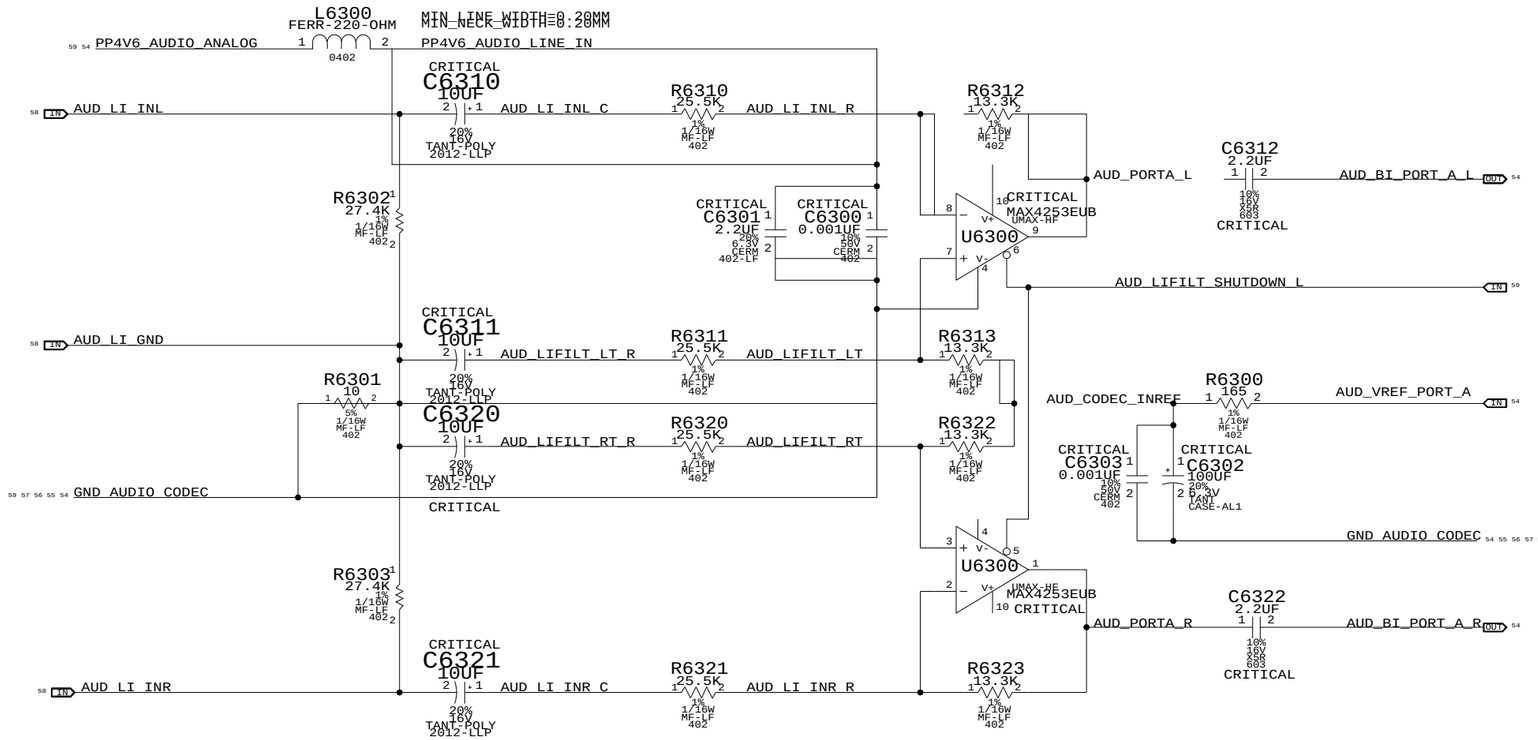
# Pseudo-Diff Line-In Filter
# GAIN = -5.4DB  AV = 0.52
# FC = 1.8 HZ




# AUDIO: LINE IN

SYNC_MASTER=AUDIO  SYNC_DATE=07/09/2008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|---|---|---|
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| SCALE: NONE | SHT 63 OF 109 | |

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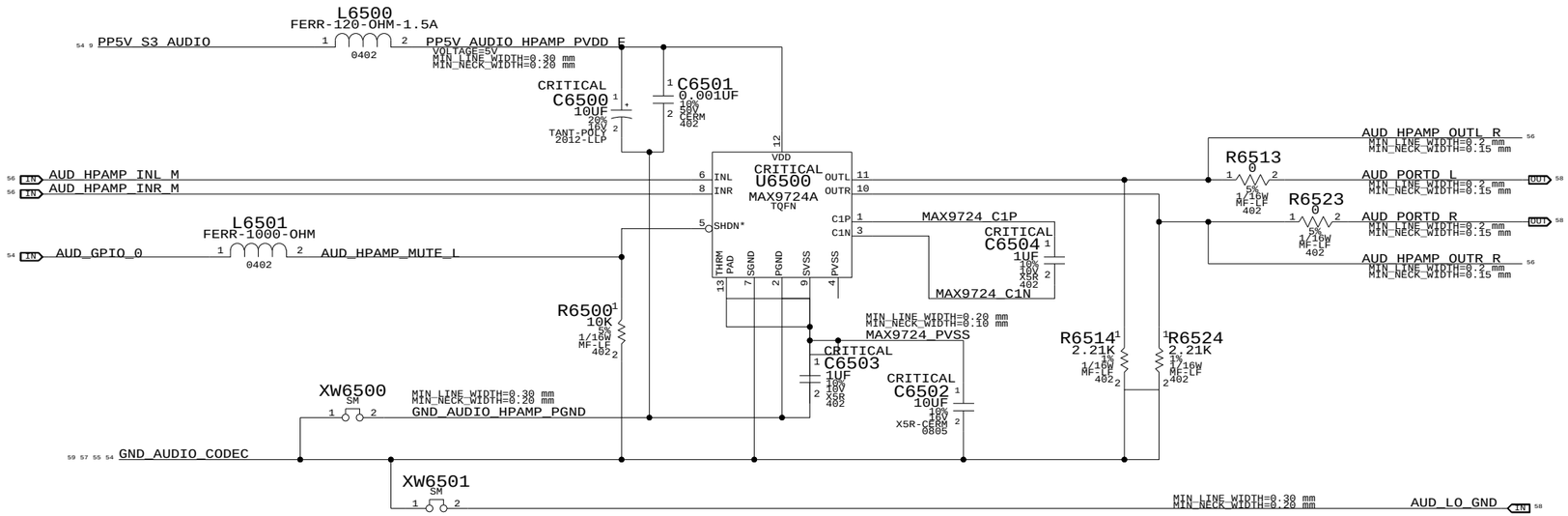
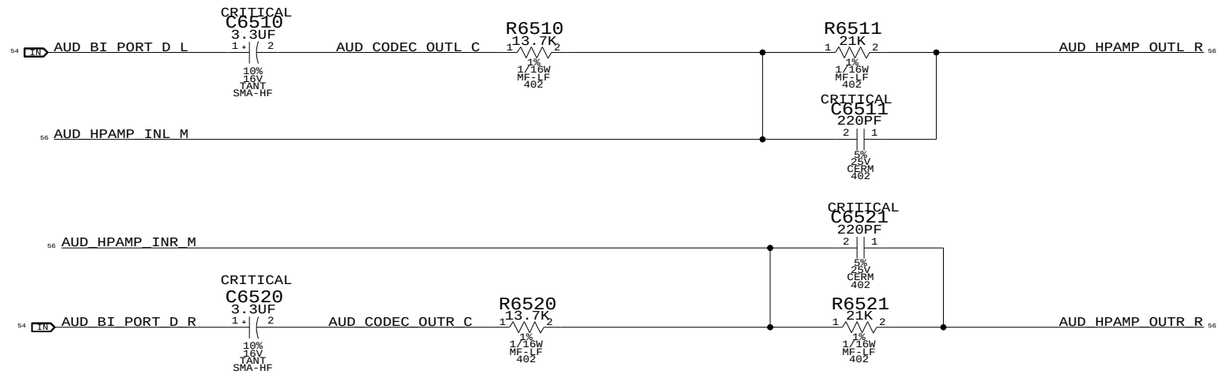
# Headphone Amplifier (MAX9724A)
# APN:353S1637




# 1st Order DAC Filter

## HP:3.52 HZ  LP:34 KHZ
## VOLTAGE GAIN:1.53




## AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO  SYNC_DATE=07/09/2008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| SCALE: NONE | SHT 65 OF 109 | |

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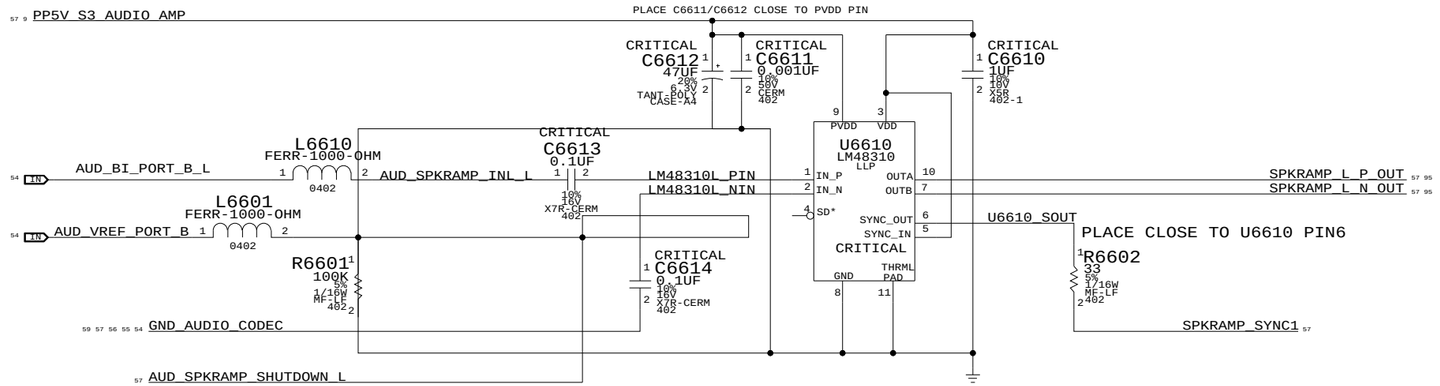
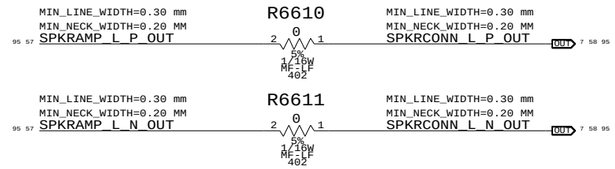
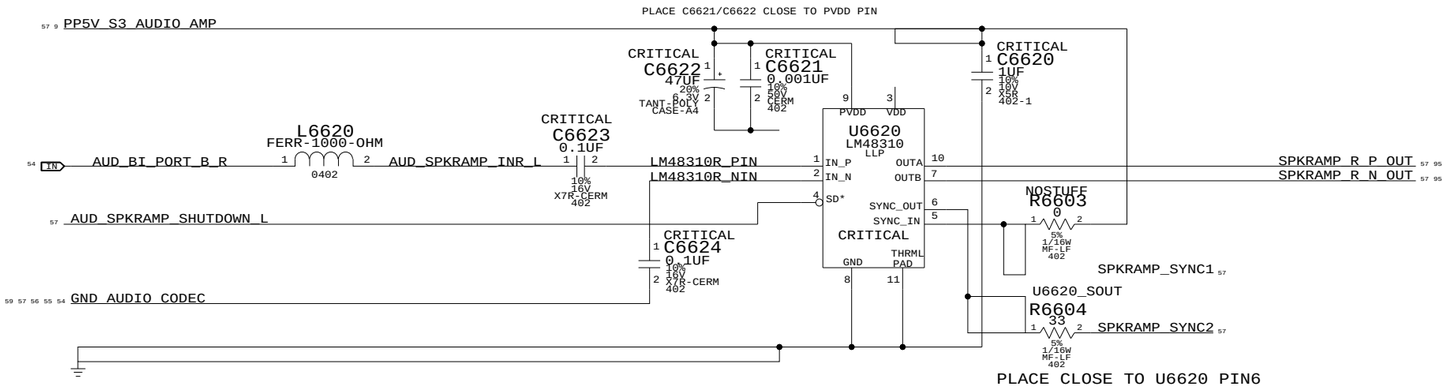
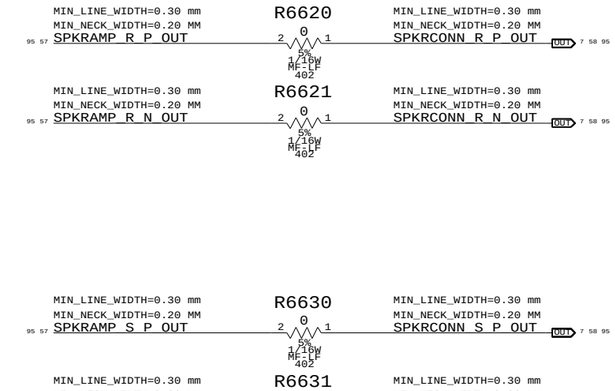
# 2X MONO SPEAKER AMPLIFIERS (LM48310)
APN: 353S1901
GAIN = 12DB
79Hz < FC (L&R) < 93Hz
53Hz < FC (SUB) < 62Hz

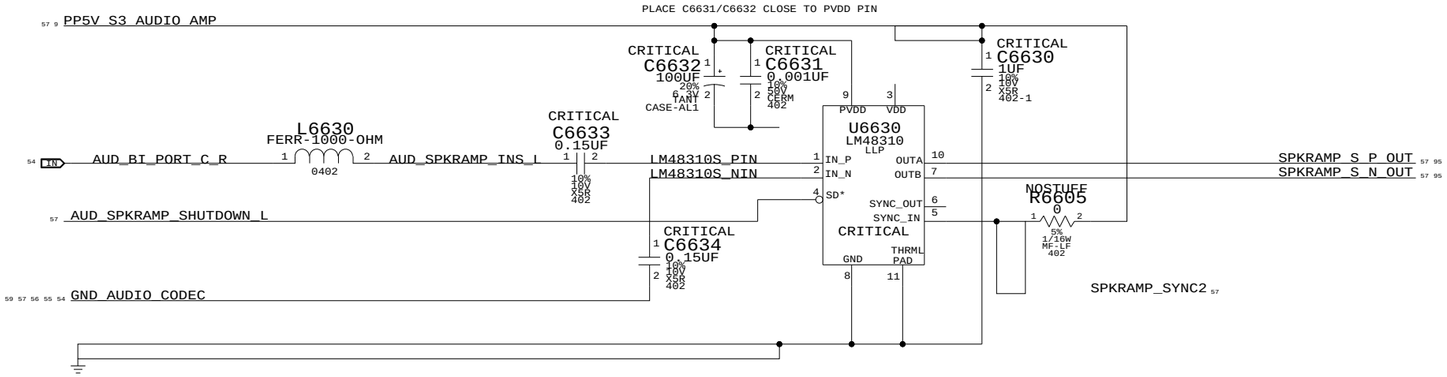


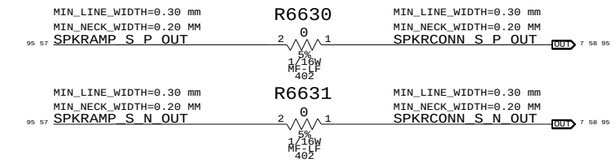

## SPEAKER CHECKPOINTS




# AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008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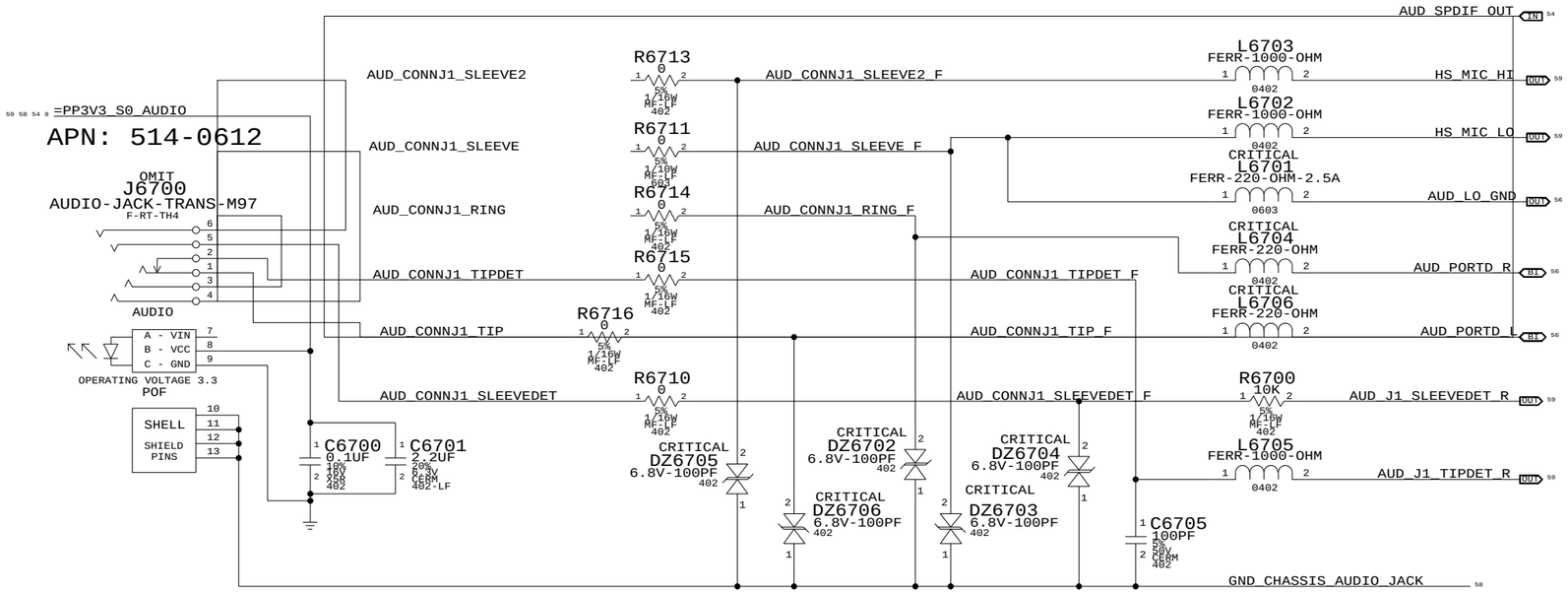
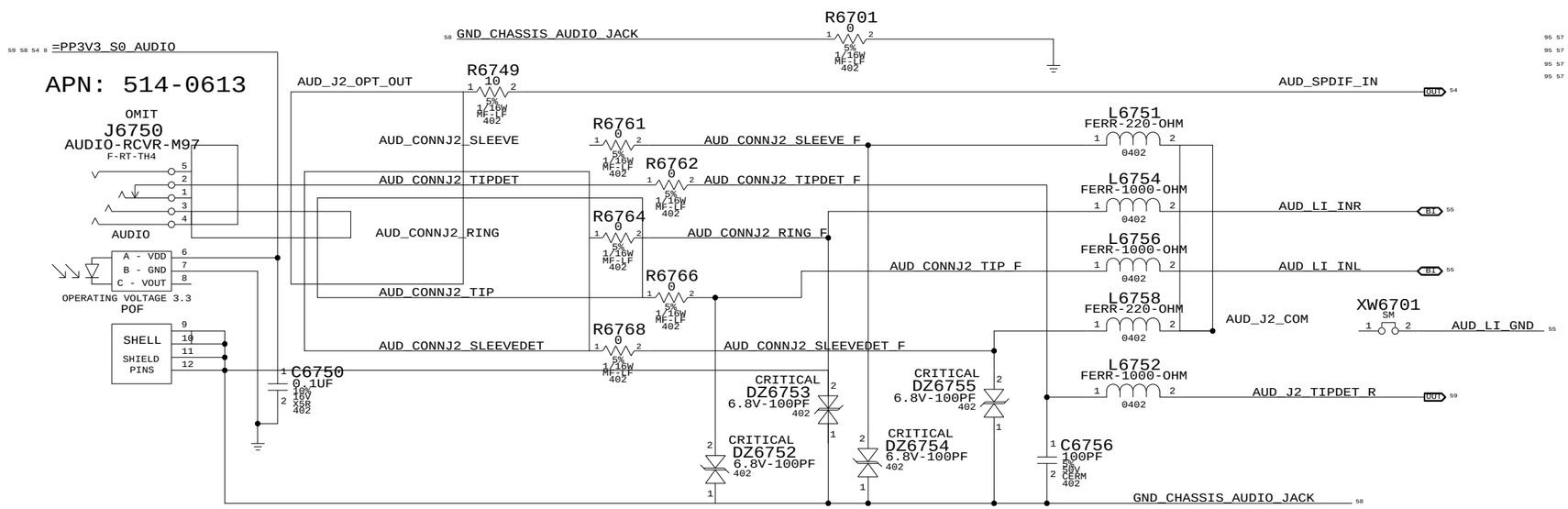
# AUDIO JACK 1 LO/HP JACK, SPDIF TX



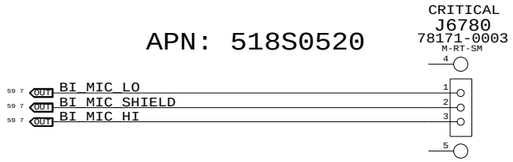

## RETURN FOR HF NOISE




# AUDIO JACK 2 LINE IN JACK, SPDIF RX

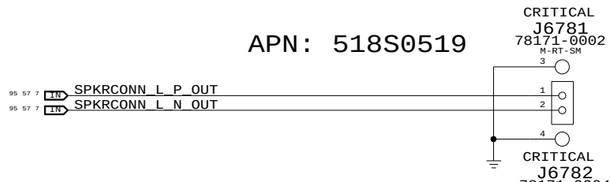
## MIC CONNECTOR

APN: 518S0520

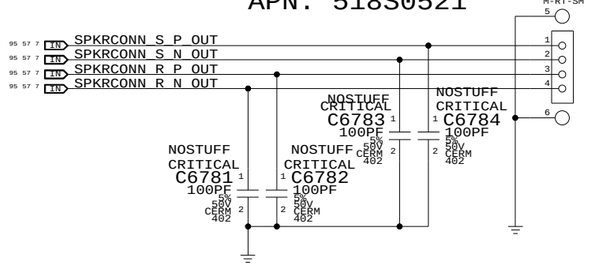



## SPEAKER CONNECTOR

APN: 518S0519




APN: 518S0521


SPKRCONN_S_P_OUT
SPKRCONN_S_N_OUT
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT
NOSTUFF CRITICAL C6783 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6781 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 100PF 5% 50V CERM 402

# AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008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| SCALE: NONE | SHT 67 OF 109 | |

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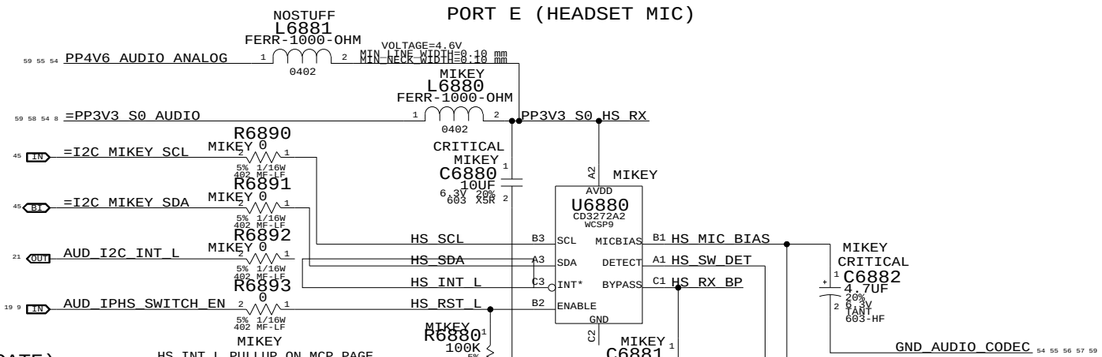
## CODEC OUTPUT SIGNAL PATHS

| FUNCTION | VOLUME | CONVERTER | MIXER(OUTPUT) | PIN COMPLEX | MUTE CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|---|---|
| HP/LINE OUT | 0X0C (12) | 0X02 (2) | 0X0C (12) | 0X14 (20,D) | GPIO_0 | 0X14 (20,D) |
| SATELLITES | 0X0D (13) | 0X03 (3) | 0X0D (13) | 0X18 (24,B) | VREF_B (100%) | N/A |
| SUB | 0X0F (15) | 0X05 (05) | 0X0F (15) | 0X1A (26,C) | VREF_B (100%) | N/A |
| SPDIF OUT | N/A | 0X06 (6) | | 0X1E (SPDIF OUT) | N/A | 0X16 (22,G) |

## CODEC INPUT SIGNAL PATHS

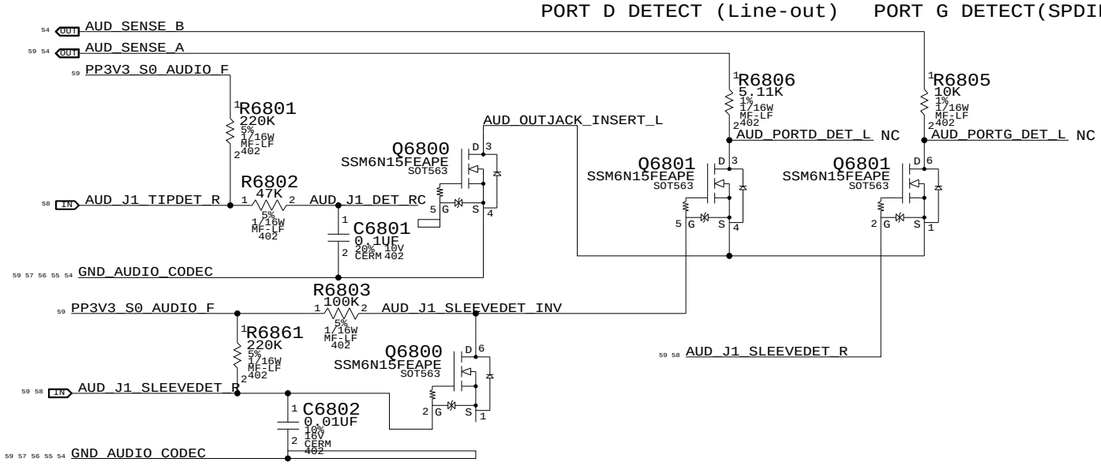
| FUNCTION | MIXER(INPUT) | CONVERTER | PIN COMPLEX | VREF | DET ASSIGNMENT |
|---|---|---|---|---|---|
| LINE IN | 0X23 (35) | 0X08 (8) | 0X15 (21,A) | VREF_A (50%) | 0X15 (21,A) |
| SPDIF IN | N/A | 0X0A (10) | 0X1F (SPDIF IN) | N/A | N/A |
| BUILT-IN MIC | 0X24 (36) | 0X07 (7) | 0X19 (25,F) | VREF_F (100%) | N/A |
| HEADSET MIC | 0X24 (36) | 0X07 (7) | 0X1B (27,E) | MIKEY | MIKEY |

## PORT E (HEADSET MIC)

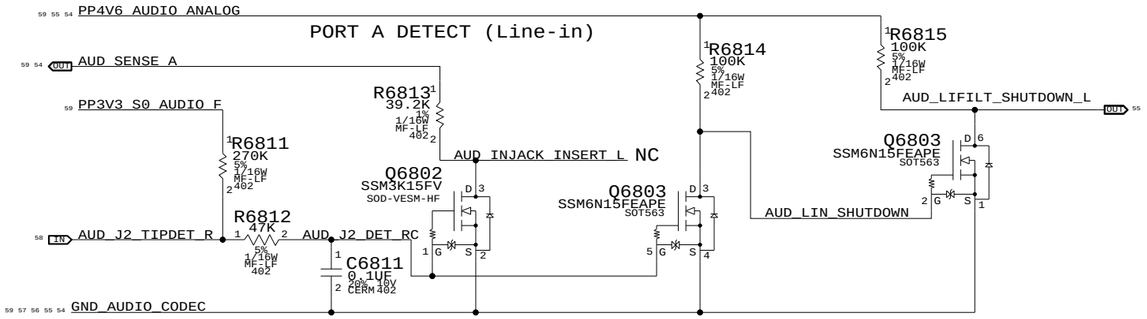



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 116S0114 | 1 | 100K 5% 0402 RESISTOR | R6883 | MIKEY |
| 132S0143 | 1 | 8200PF 10% 0402 CAPACITOR | C6884 | MIKEY |
| 131S1027 | 1 | 100PF 5% 0402 CAPACITOR | C6885 | MIKEY |
| 116S0004 | 1 | 0 OHMS 5% 0402 RESISTOR | R6883 | NOMIKEY |
| 116S0004 | 1 | 0 OHMS 5% 0402 RESISTOR | C6884 | NOMIKEY |
| 116S0004 | 1 | 0 OHMS 5% 0402 RESISTOR | C6885 | NOMIKEY |

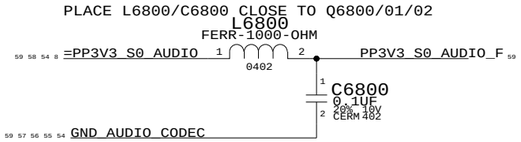
## PORT D DETECT (Line-out)  PORT G DETECT(SPDIF DELEGATE)



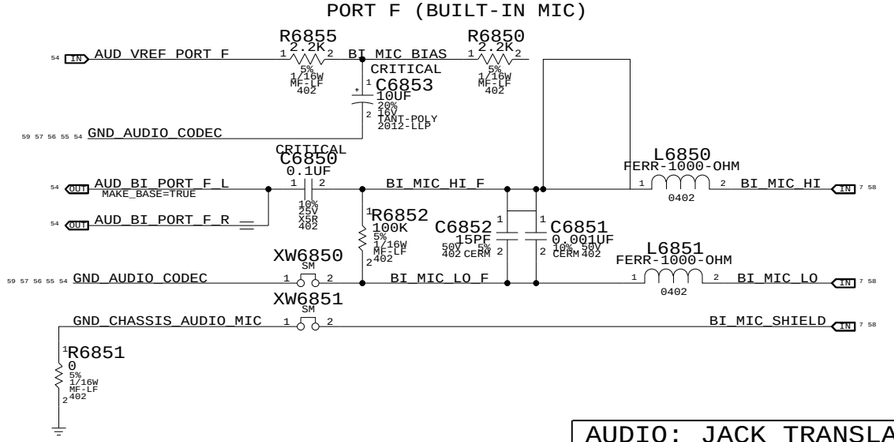

## LINE_IN AMP SHUTDOWN CONTROL




## PLACE L6800/C6800 CLOSE TO Q6800/01/02




## PORT F (BUILT-IN MIC)





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# AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO  SYNC_DATE=07/09/2008

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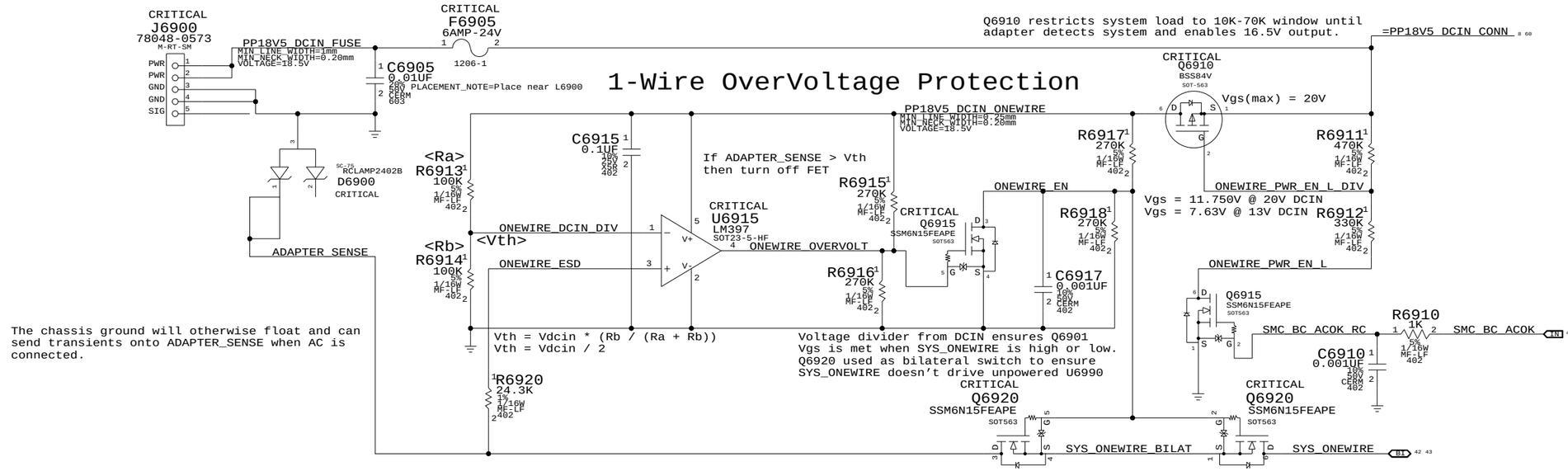
# MagSafe DC Power Jack




## DC-In & Battery Connectors

SYNC_MASTER=T18_MLB SYNC_DATE=12/06/2007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| D | 051-7902 | D |
| SCALE: NONE | SHT 69 OF 109 | |

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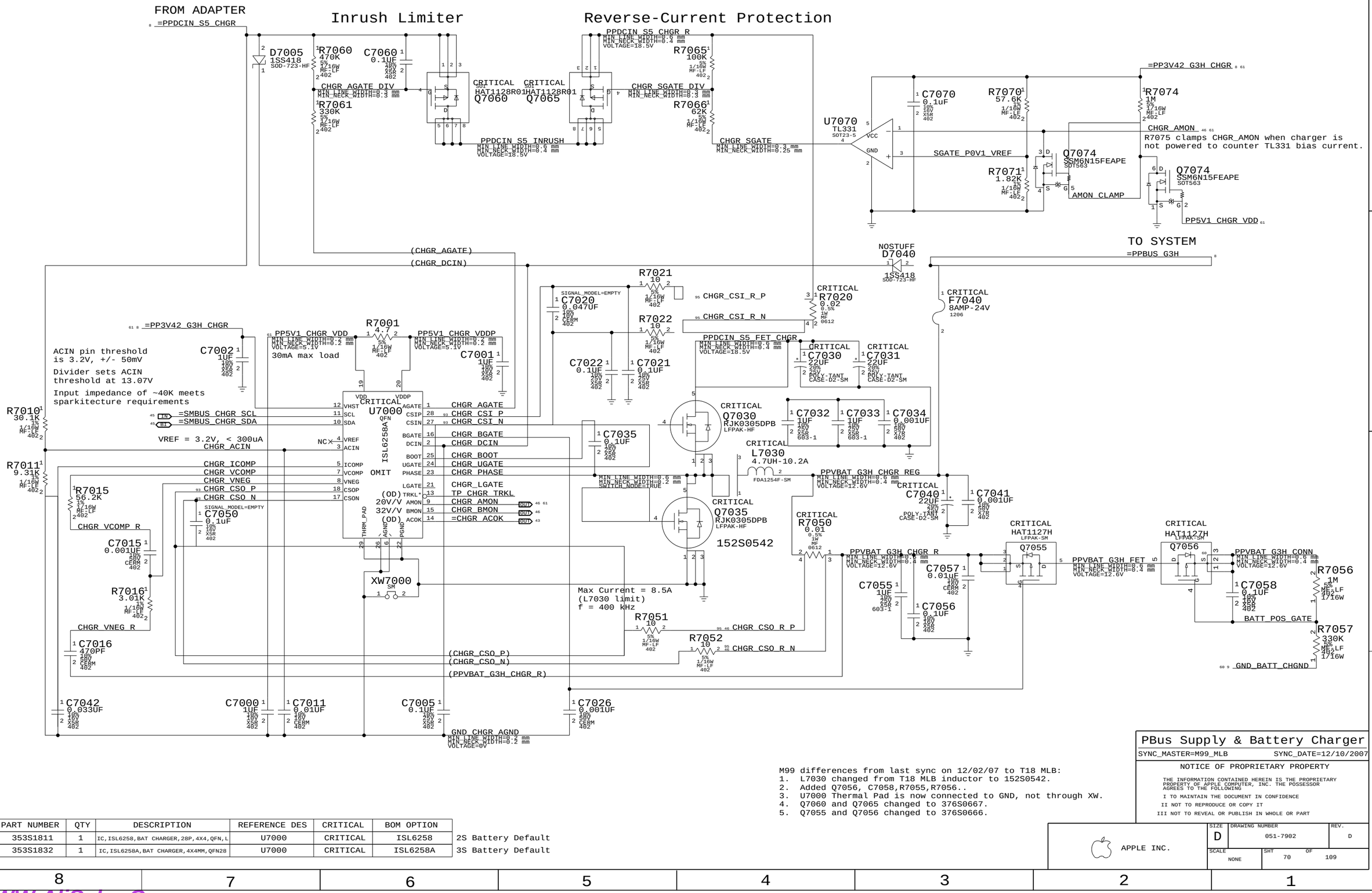


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION | |
|---|---|---|---|---|---|---|
| 353S1811 | 1 | IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L | U7000 | CRITICAL | ISL6258 | 2S Battery Default |
| 353S1832 | 1 | IC,ISL6258A,BAT CHARGER,4X4MM,QFN28 | U7000 | CRITICAL | ISL6258A | 3S Battery Default |

M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

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| D | 051-7902 | D |
| SCALE: NONE | SHT 70 OF 109 | |

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| DPRSLPVR | DPRSTP* | PSI* | Operation | Mode |
|---|---|---|---|---|
| 0 | 1 | 1 | 2-Phase | CCM |
| 0 | 1 | 0 | 1-Phase | CCM |
| 1 | 0 | 1 | 1-Phase | DCM |
| 1 | 0 | 0 | 1-Phase | DCM |

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

| IMVP_VR_ON | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
|---|---|---|
| IMVP_OCSET | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_VO | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_DROOP | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_DFB | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_SOFT | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_RBIAS | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_VDIFF | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_FB2 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_FB | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_COMP | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |
| IMVP_VW | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.20 MM |

| | | |
|---|---|---|
| IMVP_PHASE1 | MIN_LINE_WIDTH=1.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_BOOT1 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_UGATE1 | MIN_LINE_WIDTH=0.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_LGATE1 | MIN_LINE_WIDTH=0.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_ISEN1 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_VSUM1 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.25 MM |
| IMVP_VO1 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.25 MM |
| IMVP_VSEN_P | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |

| | | |
|---|---|---|
| IMVP_PHASE2 | MIN_LINE_WIDTH=1.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_BOOT2 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_UGATE2 | MIN_LINE_WIDTH=0.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_LGATE2 | MIN_LINE_WIDTH=0.5 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_ISEN2 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |
| IMVP_VSUM2 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.25 MM |
| IMVP_VO2 | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.25 MM |
| IMVP_VSEN_N | MIN_LINE_WIDTH=0.25 MM | MIN_NECK_WIDTH=0.2 MM |

# IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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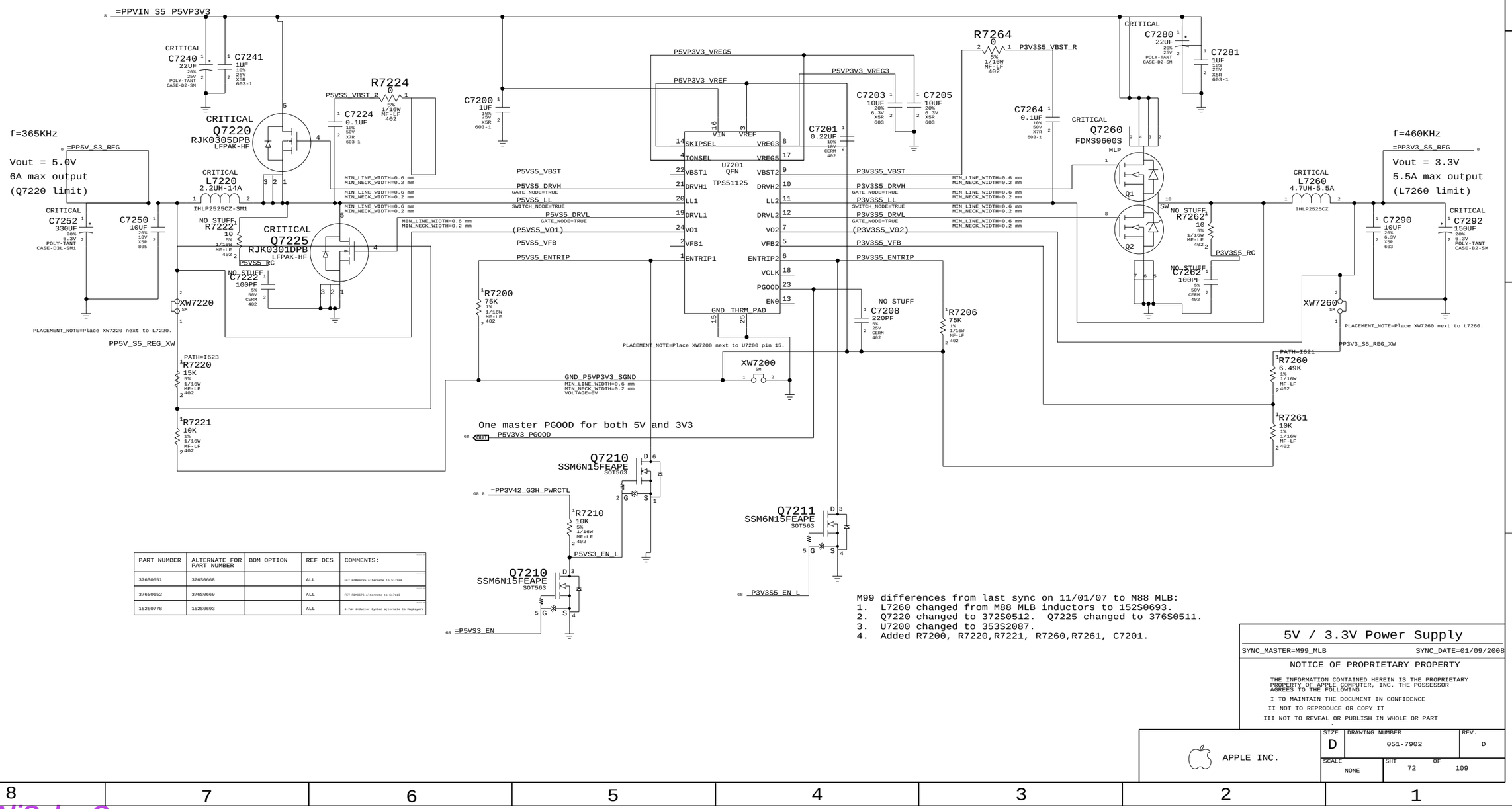


| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 376S0651 | 376S0668 | | ALL | FET FDMS8676S alternate to Si7540 |
| 376S0652 | 376S0669 | | ALL | FET FDMS8670 alternate to Si7510 |
| 152S0778 | 152S0693 | | ALL | 4.7uH inductor Cyntec alternate to Magnayers |

M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220,R7221, R7260,R7261, C7201.

# 5V / 3.3V Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=01/09/2008


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| SCALE | SHT | OF |
| NONE | 72 | 109 |

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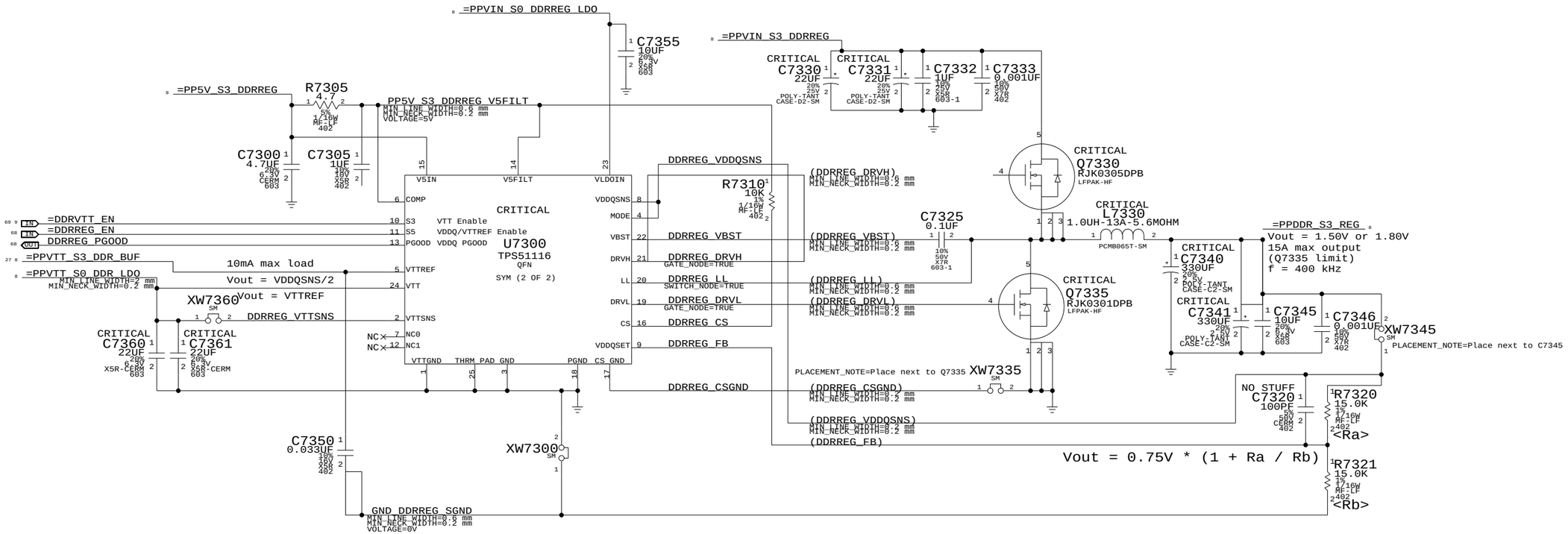


# 1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007


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| SCALE | SHT | OF |
|---|---|---|
| NONE | 73 | 109 |

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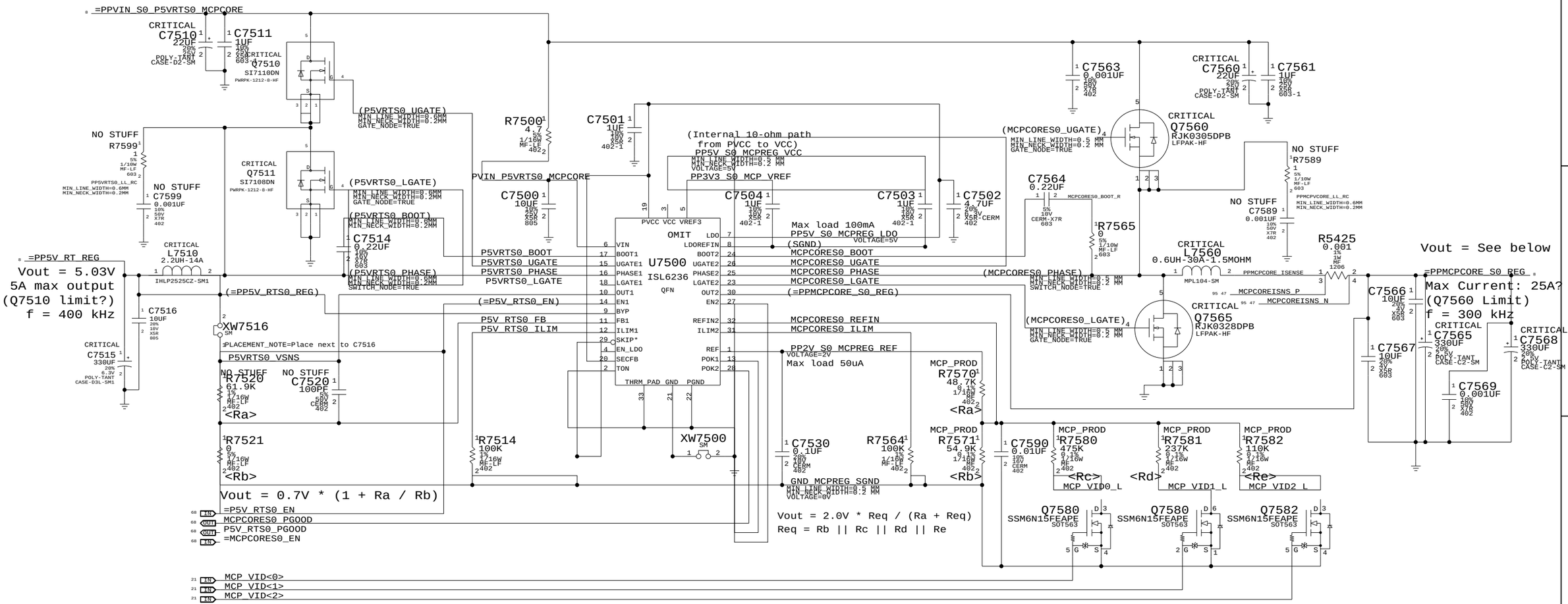
=PPVIN_S0_P5VRTS0_MCPCORE
CRITICAL C7510 22UF 20% 25V POLY-TANT CASE-D2-SM
C7511 1UF 10% 25V X5R 603-1
CRITICAL Q7510 SI7116DN PWRPK-1212-8-HF
(P5VRTS0_UGATE) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM GATE_NODE=TRUE
NO STUFF R7599 1 5% 1/10W MF-LF 603
PP5VRTS0_LL_RC MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
NO STUFF C7599 0.001UF 10% 50V X7R 402
CRITICAL Q7511 SI7108DN PWRPK-1212-8-HF
(P5VRTS0_LGATE) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM GATE_NODE=TRUE
(P5VRTS0_BOOT) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C7514 0.22UF 10% 16V X7R 603
(P5VRTS0_PHASE) MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM SWITCH_NODE=TRUE
R7500 4.7 5% 1/10W MF-LF 402
C7501 1UF 10% 16V X5R 402-1
PVIN_P5VRTS0_MCPCORE
C7500 10UF 10% 25V X5R 805
(Internal 10-ohm path from PVCC to VCC)
PP5V_S0_MCPREG_VCC MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
PP3V3_S0_MCP_VREF
C7504 1UF 10% 16V X5R 402-1
C7503 1UF 10% 16V X5R 402-1
C7502 4.7UF 20% 6.3V X5R-CERM 402
C7563 0.001UF 10% 50V X7R 402
CRITICAL C7560 22UF 20% 25V POLY-TANT CASE-D2-SM
C7561 1UF 10% 25V X5R 603-1
(MCPCORES0_UGATE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM GATE_NODE=TRUE
CRITICAL Q7560 RJK0305DPB LFPAK-HF
NO STUFF R7589 1 5% 1/10W MF-LF 603
C7564 0.22UF 5% 10V CERM-X7R 603
MCPCORES0_BOOT_R
R7565 0 5% 1/10W MF-LF 603
NO STUFF C7589 0.001UF 10% 50V X7R 402
PPMCPVCORE_LL_RC MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
R5425 0.001 1% 1W MF 1206
Vout = See below
=PPMCPCORE_S0_REG
Max Current: 25A?
(Q7560 Limit)
f = 300 kHz
CRITICAL L7560 0.6UH-30A-1.5MOHM MPL104-SM
PPMCPCORE_ISENSE
MCPCOREISNS_P
MCPCOREISNS_N
(MCPCORES0_PHASE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM SWITCH_NODE=TRUE
(MCPCORES0_LGATE) MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM GATE_NODE=TRUE
CRITICAL Q7565 RJK0328DPB LFPAK-HF
C7566 10UF 20% 4V X5R 603
C7567 10UF 20% 4V X5R 603
CRITICAL C7565 330UF 20% 2.5V POLY-TANT CASE-C2-SM
CRITICAL C7568 330UF 20% 2.5V POLY-TANT CASE-C2-SM
C7569 0.001UF 10% 50V X7R 402
=PP5V_RT_REG
Vout = 5.03V
5A max output
(Q7510 limit?)
f = 400 kHz
CRITICAL L7510 2.2UH-14A IHLP2525CZ-SM1
C7516 10UF 20% 10V X5R 805
CRITICAL C7515 330UF 20% 6.3V POLY-TANT CASE-D3L-SM1
(=PP5V_RTS0_REG)
XW7516 SM
PLACEMENT_NOTE=Place next to C7516
P5VRTS0_VSNS
NO STUFF R7520 61.9K 1% 1/16W MF-LF 402 <Ra>
NO STUFF C7520 100PF 5% 50V CERM 402
R7521 0 5% 1/16W MF-LF 402 <Rb>
Vout = 0.7V * (1 + Ra / Rb)
R7514 100K 1% 1/16W MF-LF 402
XW7500 SM
C7530 0.1UF 20% 10V CERM 402
GND_MCPREG_SGND MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V
R7564 100K 1% 1/16W MF-LF 402
MCP_PROD R7570 48.7K 1% 1/16W 402 <Ra>
MCP_PROD R7571 54.9K 1% 1/16W 402 <Rb>
Vout = 2.0V * Req / (Ra + Req)
Req = Rb || Rc || Rd || Re
C7590 0.01UF 10% 16V CERM 402
MCP_PROD R7580 475K 1% 1/16W 402 <Rc> MCP_VID0_L
MCP_PROD R7581 237K 1% 1/16W 402 <Rd> MCP_VID1_L
MCP_PROD R7582 110K 1% 1/16W 402 <Re> MCP_VID2_L
Q7580 SSM6N15FEAPE SOT563
Q7580 SSM6N15FEAPE SOT563
Q7582 SSM6N15FEAPE SOT563
U7500 ISL6236 QFN
OMIT
VIN BOOT1 UGATE1 PHASE1 LGATE1 OUT1 EN1 BYP FB1 ILIM1 SKIP* EN_LDO SECFB TON
LDO LDOREFIN BOOT2 UGATE2 PHASE2 LGATE2 OUT2 EN2 REFIN2 ILIM2 REF POK1 POK2
PVCC VCC VREF3 THRM_PAD GND PGND
Max load 100mA
PP5V_S0_MCPREG_LDO VOLTAGE=5V
(SGND)
P5VRTS0_BOOT
P5VRTS0_UGATE
P5VRTS0_PHASE
P5VRTS0_LGATE
(=P5V_RTS0_EN)
P5V_RTS0_FB
P5V_RTS0_ILIM
MCPCORES0_BOOT
MCPCORES0_UGATE
MCPCORES0_PHASE
MCPCORES0_LGATE
(=PPMCPCORE_S0_REG)
MCPCORES0_REFIN
MCPCORES0_ILIM
PP2V_S0_MCPREG_REF VOLTAGE=2V
Max load 50uA
=P5V_RTS0_EN
MCPCORES0_PGOOD
P5V_RTS0_PGOOD
=MCPCORES0_EN
MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
MCP79 Rev A01 requires higher core & analog voltage

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0382 | 1 | RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF | R7570 | | MCP_A01 |
| 114S0400 | 1 | RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF | R7571 | | MCP_A01 |
| 114S0482 | 1 | RES,MTL FILM,1/16W,523K,1,0402,SMD,LF | R7580 | | MCP_A01 |
| 114S0453 | 1 | RES,MTL FILM,1/16W,267K,1,0402,SMD,LF | R7581 | | MCP_A01 |
| 114S0422 | 1 | RES,MTL FILM,1/16W,130K,1,0402,SMD,LF | R7582 | | MCP_A01 |
| 114S0373 | 1 | RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF | R7570 | | MCP_A01Q |
| 114S0404 | 1 | RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF | R7571 | | MCP_A01Q |
| 114S0458 | 1 | RES,MTL FILM,1/16W,301K,1,0402,SMD,LF | R7580 | | MCP_A01Q |
| 114S0447 | 1 | RES,MTL FILM,1/16W,237K,1,0402,SMD,LF | R7581 | | MCP_A01Q |
| 114S0411 | 1 | RES,MTL FILM,1/16W,100K,1,0402,SMD,LF | R7582 | | MCP_A01Q |

| VID<2:0> | Rev A01 Voltage | Production Voltage | MCP Target |
|---|---|---|---|
| 000 | +1.224V | +1.060V | +1.05V |
| 001 | +1.159V | +0.994V | +1.00V |
| 010 | +1.101V | +0.937V | +0.95V |
| 011 | +1.049V | +0.885V | +0.90V |
| 100 | +0.995V | +0.830V | +0.85V |
| 101 | +0.952V | +0.789V | +0.80V |
| 110 | +0.913V | +0.752V | +0.75V |
| 111 | +0.876V | +0.719V | +0.70V |

5V_S0 / MCP Core Regulator

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 75 OF 109 | |

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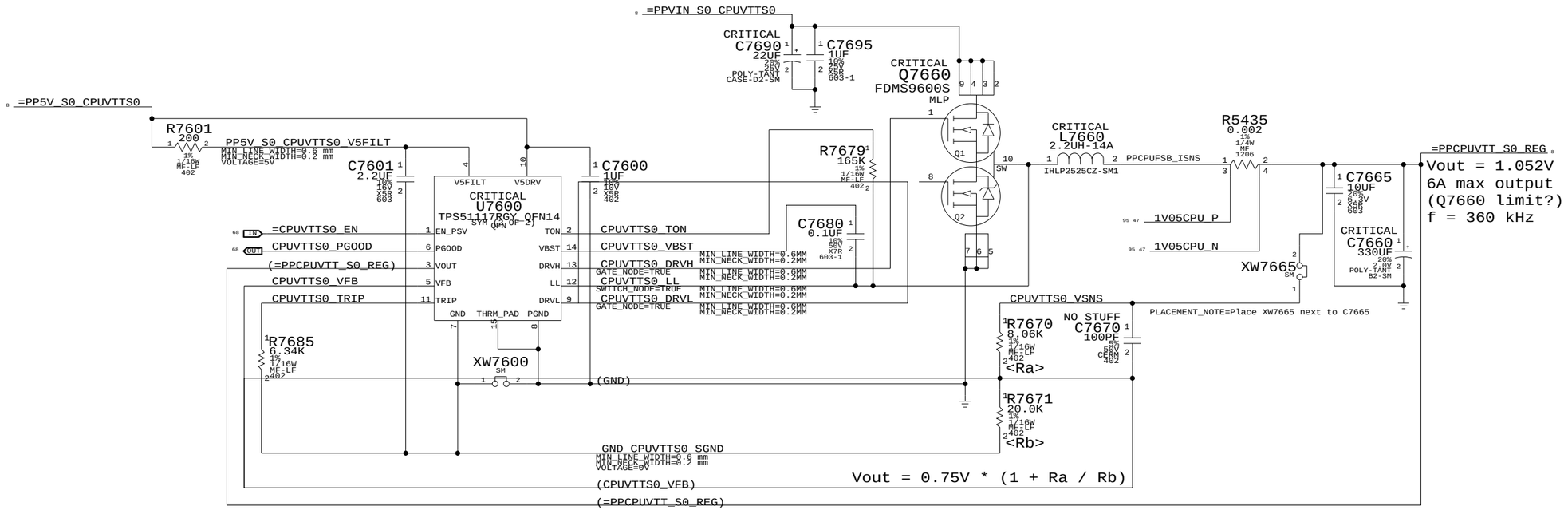


M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

# CPU VTT Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007


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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 76 OF 109 | |

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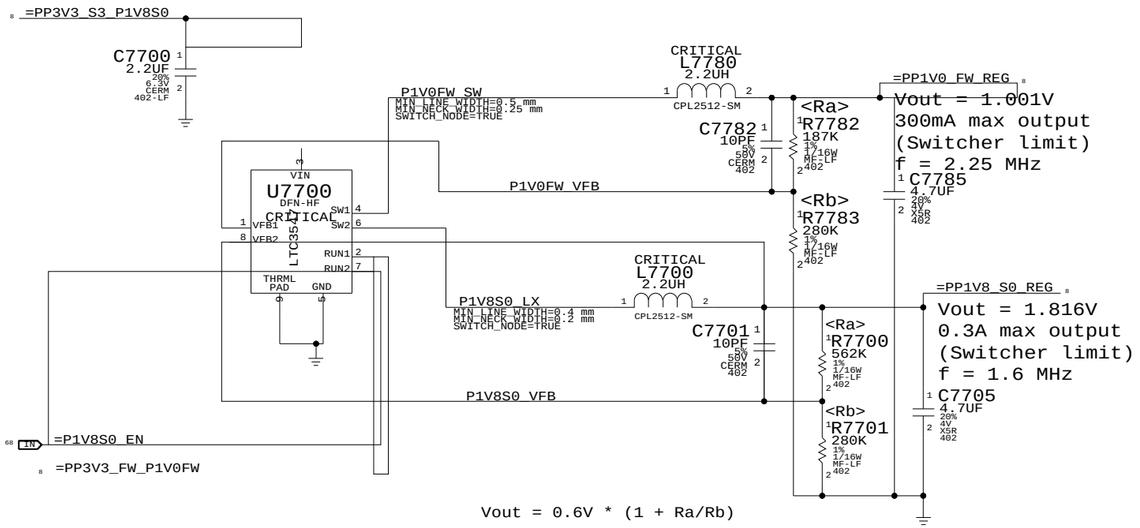
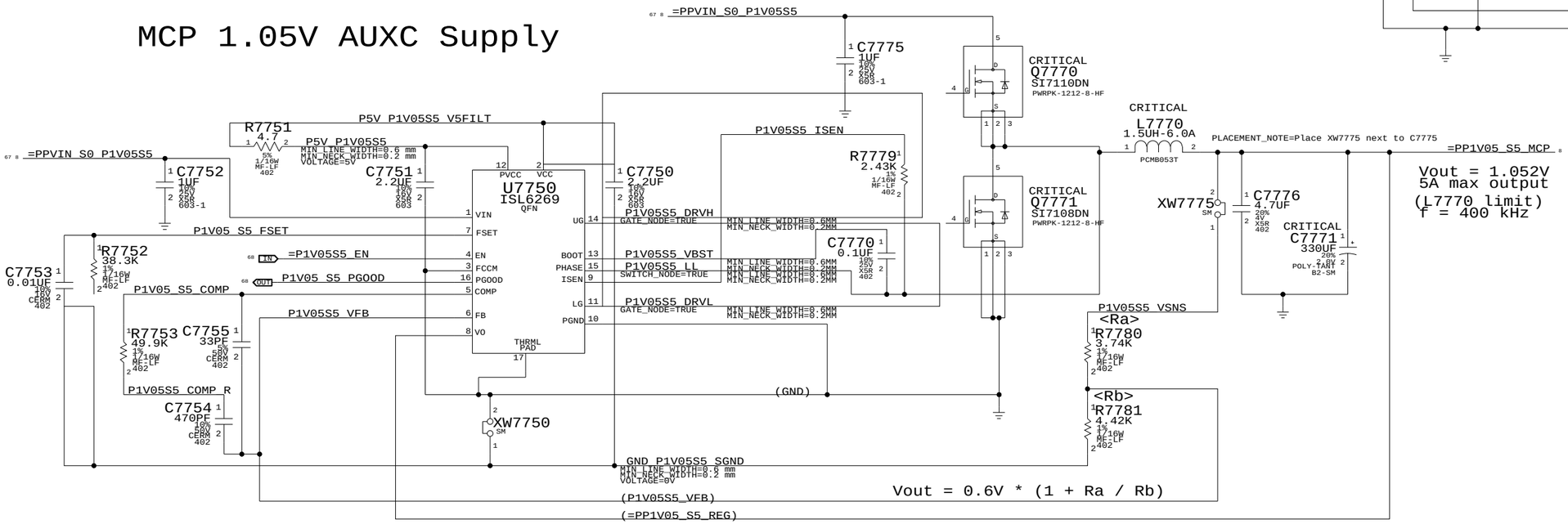
# 1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature



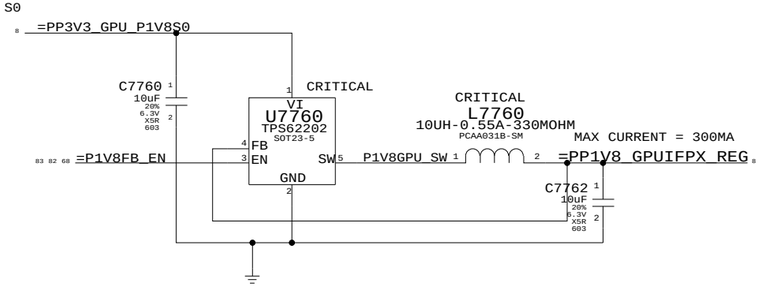

Vout = 0.6V * (1 + Ra/Rb)

# MCP 1.05V AUXC Supply




# 1.8V S0 Switcher

INPUT RAIL IS 3.3V S0




Misc Power Supplies

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 77 OF 109 | |

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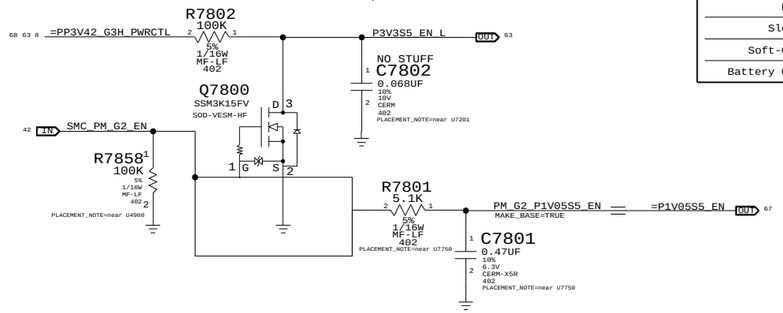
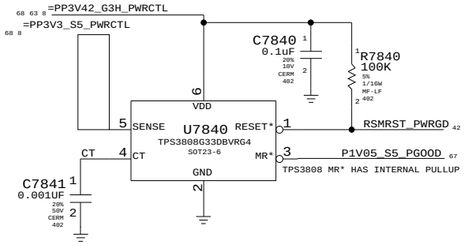
## 3.3V 1,05V S5 ENABLE

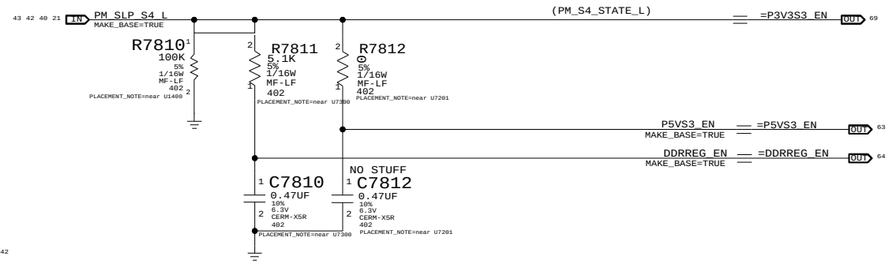

R7802 100K 5% 1/16W MF-LF 402
=PP3V42_G3H_PWRCTL
P3V3S5_EN_L
NO STUFF C7802 0.068UF 10% 10V CERM 402 PLACEMENT_NOTE=near U7201
Q7800 SSM3K15FV SOD-VESM-HF
SMC_PM_G2_EN
R7858 100K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U4900
R7801 5.1K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7750
PM_G2_P1V05S5_EN MAKE_BASE=TRUE
=P1V05S5_EN
C7801 0.47UF 10% 6.3V CERM-X5R 402 PLACEMENT_NOTE=near U7750

| State | SMC_PM_G2_ENABLE | PM_SLP_S4_L | PM_SLP_S3_L |
|---|---|---|---|
| Run (S0) | 1 | 1 | 1 |
| Sleep (S3) | 1 | 1 | 0 |
| Soft-Off (S5) | 1 | 0 | 0 |
| Battery Off (G3Hot) | 0 | 0 | 0 |

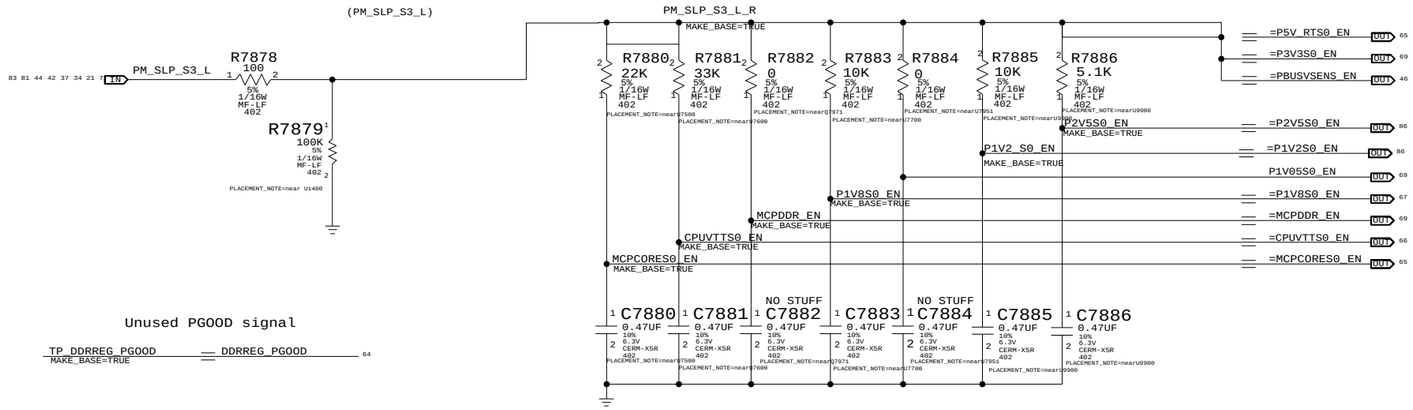
## S5 rail PWRGD




## 3.3V,5V S3 ENABLE

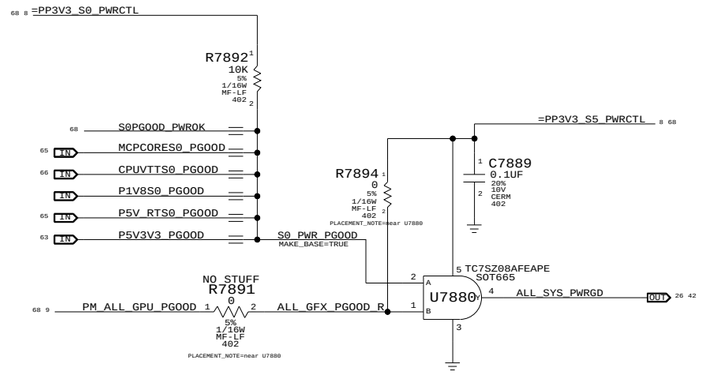

PM_SLP_S4_L MAKE_BASE=TRUE
R7810 100K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U1400
(PM_S4_STATE_L)
=P3V3S3_EN
R7811 5.1K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7300
R7812 0 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7201
P5VS3_EN MAKE_BASE=TRUE
=P5VS3_EN
DDRREG_EN MAKE_BASE=TRUE
=DDRREG_EN
C7810 0.47UF 10% 6.3V CERM-X5R 402 PLACEMENT_NOTE=near U7300
NO STUFF C7812 0.47UF 10% 6.3V CERM-X5R 402 PLACEMENT_NOTE=near U7201

## S0 ENABLE


(PM_SLP_S3_L)
PM_SLP_S3_L
R7878 100 5% 1/16W MF-LF 402
R7879 100K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U1400
PM_SLP_S3_L_R MAKE_BASE=TRUE
R7880 22K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7500
R7881 33K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7600
R7882 0 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7971
R7883 10K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7700
R7884 0 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U7951
R7885 10K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U9500
R7886 5.1K 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U9900
=P5V_RTS0_EN
=P3V3S0_EN
=PBUSVSENS_EN
P2V5S0_EN MAKE_BASE=TRUE
=P2V5S0_EN
P1V2_S0_EN MAKE_BASE=TRUE
=P1V2S0_EN
P1V05S0_EN
P1V8S0_EN MAKE_BASE=TRUE
=P1V8S0_EN
MCPDDR_EN MAKE_BASE=TRUE
=MCPDDR_EN
CPUVTTS0_EN MAKE_BASE=TRUE
=CPUVTTS0_EN
MCPCORES0_EN MAKE_BASE=TRUE
=MCPCORES0_EN
C7880 0.47UF 10% 6.3V CERM-X5R 402
C7881 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7882 0.47UF 10% 6.3V CERM-X5R 402
C7883 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7884 0.47UF 10% 6.3V CERM-X5R 402
C7885 0.47UF 10% 6.3V CERM-X5R 402
C7886 0.47UF 10% 6.3V CERM-X5R 402

## Other S0 RAILS

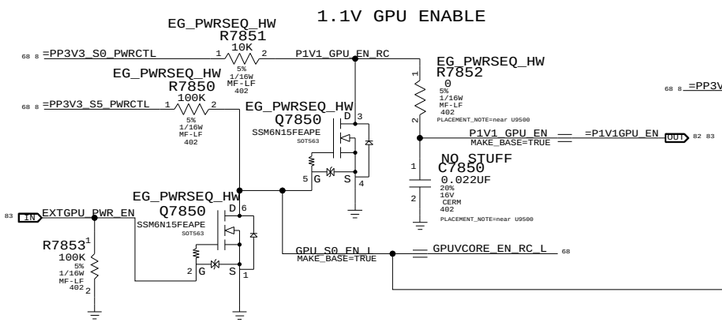
| | PM_ALL_GFX_PGOOD |
|---|---|
| IG | high |
| EG | PM_ALL_GPU_PGOOD |



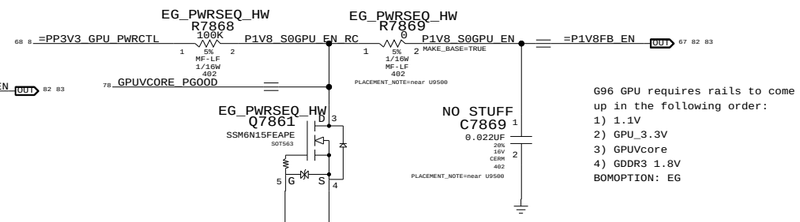

## Unused PGOOD signal




## 1.1V GPU ENABLE



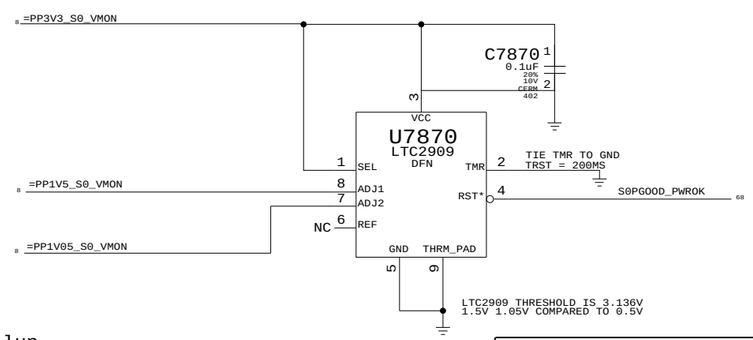

## Graphic MEM ENABLE


EG_PWRSEQ_HW R7868 100K 5% 1/16W MF-LF 402
=PP3V3_GPU_PWRCTL
P1V8_S0GPU_EN_RC
EG_PWRSEQ_HW R7869 0 5% 1/16W MF-LF 402 PLACEMENT_NOTE=near U9500
P1V8_S0GPU_EN MAKE_BASE=TRUE
=P1V8FB_EN
GPUVCORE_PGOOD
EG_PWRSEQ_HW Q7861 SSM6N15FEAPE SOT563
NO STUFF C7869 0.022UF 20% 16V CERM 402 PLACEMENT_NOTE=near U9500

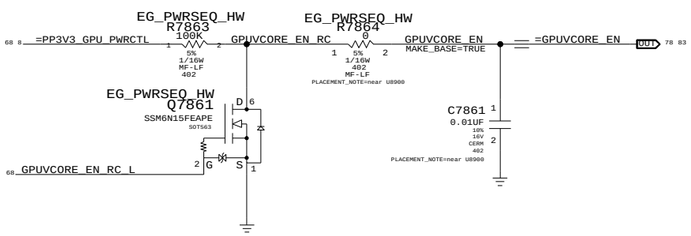
G96 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUVcore
4) GDDR3 1.8V
BOMOPTION: EG

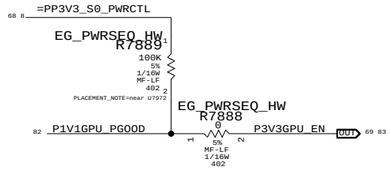
## 3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XW0402 if needed to save trace space for pin 7,8

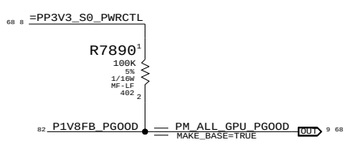



## GPUVCORE ENABLE




## EXT GPU PWRGD Pullup




Power Control

SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 78 OF 109 | |

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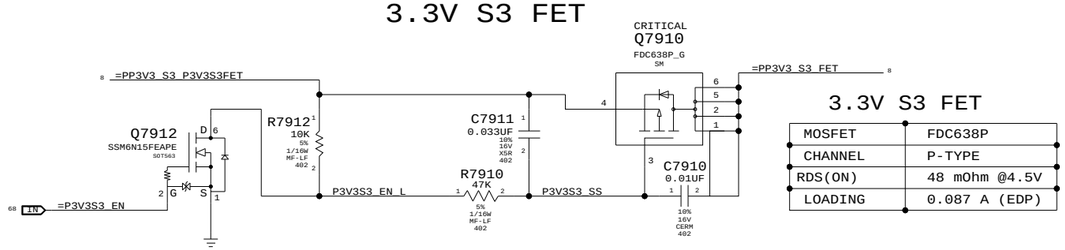
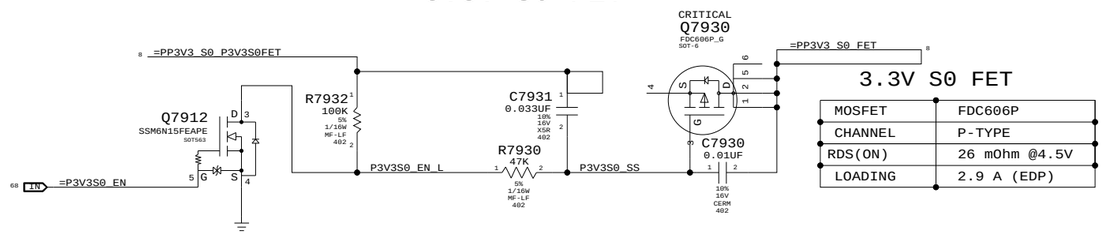
## 3.3V S3 FET



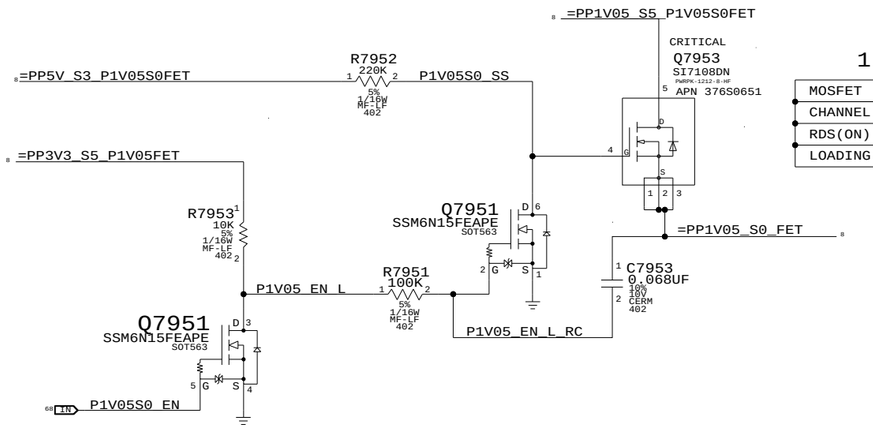

| 3.3V S3 FET | |
|---|---|
| MOSFET | FDC638P |
| CHANNEL | P-TYPE |
| RDS(ON) | 48 mOhm @4.5V |
| LOADING | 0.087 A (EDP) |

## 3.3V S0 FET



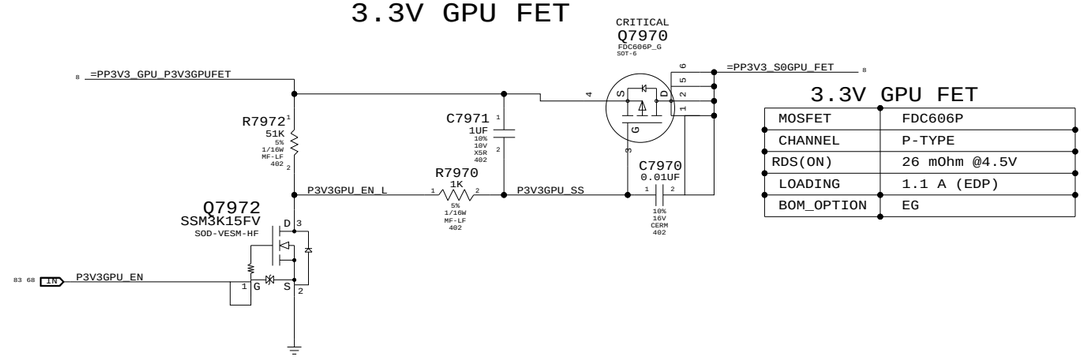

| 3.3V S0 FET | |
|---|---|
| MOSFET | FDC606P |
| CHANNEL | P-TYPE |
| RDS(ON) | 26 mOhm @4.5V |
| LOADING | 2.9 A (EDP) |

## 1.05V S0 FET



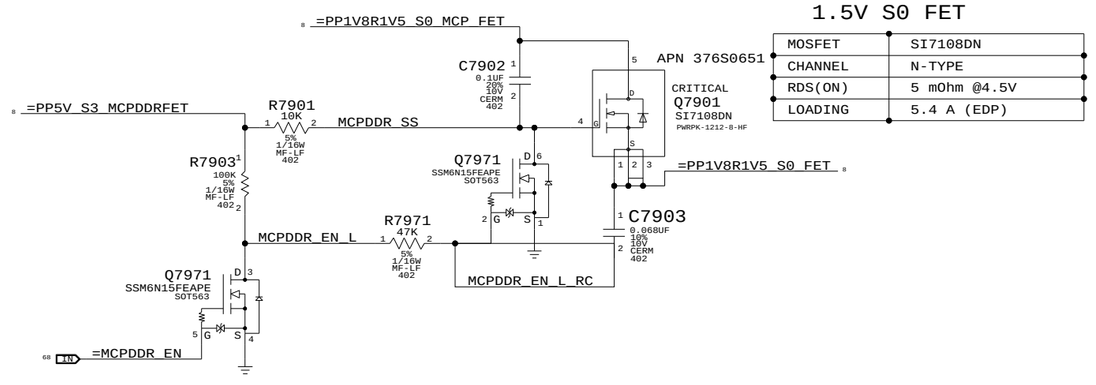

| 1.05V S0 FET | |
|---|---|
| MOSFET | SI7108DN |
| CHANNEL | N-TYPE |
| RDS(ON) | 5 mOhm @4.5V |
| LOADING | 2.1 A (EDP) |

## 3.3V GPU FET




| 3.3V GPU FET | |
|---|---|
| MOSFET | FDC606P |
| CHANNEL | P-TYPE |
| RDS(ON) | 26 mOhm @4.5V |
| LOADING | 1.1 A (EDP) |
| BOM_OPTION | EG |

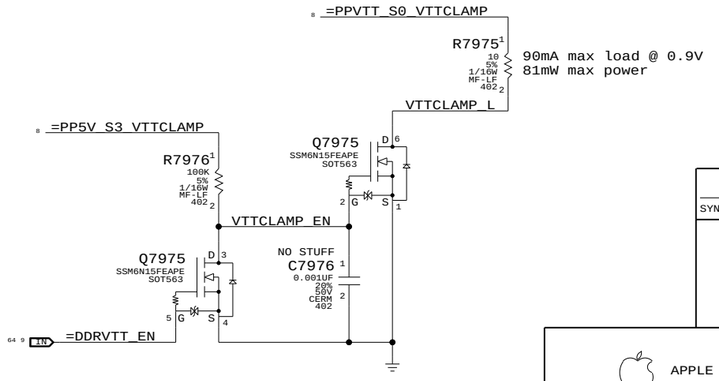
## 1.5V S0 FET




| 1.5V S0 FET | |
|---|---|
| MOSFET | SI7108DN |
| CHANNEL | N-TYPE |
| RDS(ON) | 5 mOhm @4.5V |
| LOADING | 5.4 A (EDP) |

## MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.




| Power FETs | |
|---|---|
| SYNC_MASTER=PWRSQNC | SYNC_DATE=05/12/2008 |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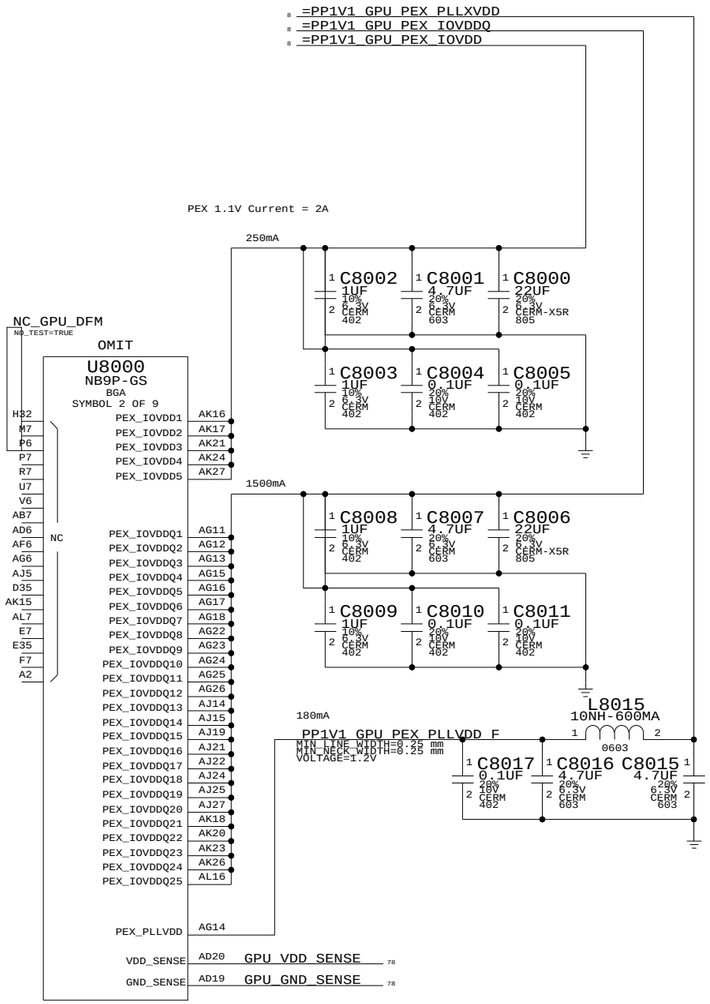
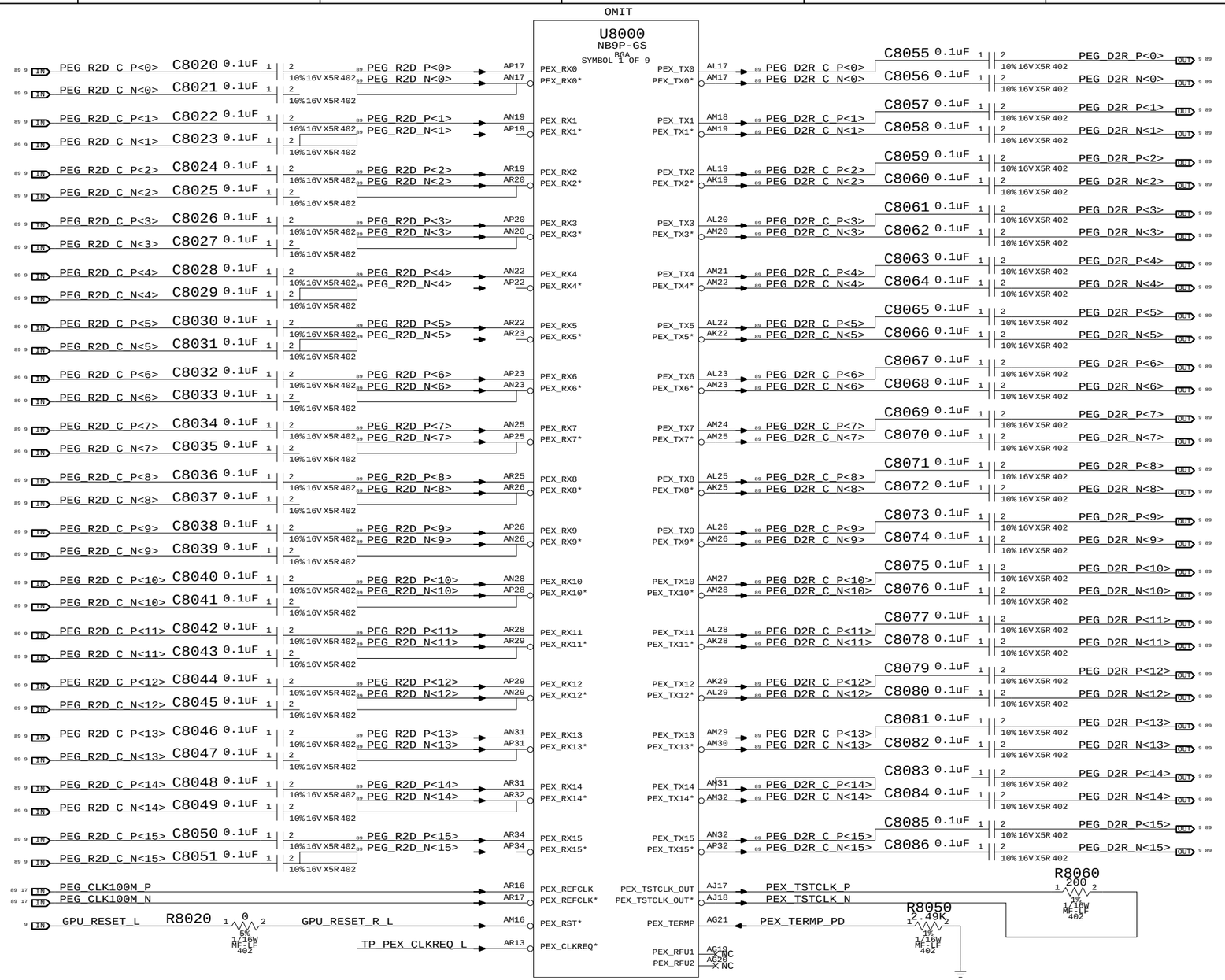
# Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)




## NV G96 PCI-E

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008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# Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V XSR-CERM 402
C8101 4.7UF 20% 6.3V XSR-CERM 402
C8102 4.7UF 20% 6.3V XSR-CERM 402

C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402

C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402

C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402

C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 9 OF 9

L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

VDD

V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

VDD

U8000
NB9P-GS
BGA
SYMBOL 8 OF 9

B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

GND

GND

V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30

=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603

C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402

C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402

C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 7 OF 9

B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

FBVDDQ

J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

FBVDDQ

NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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| NONE | | |

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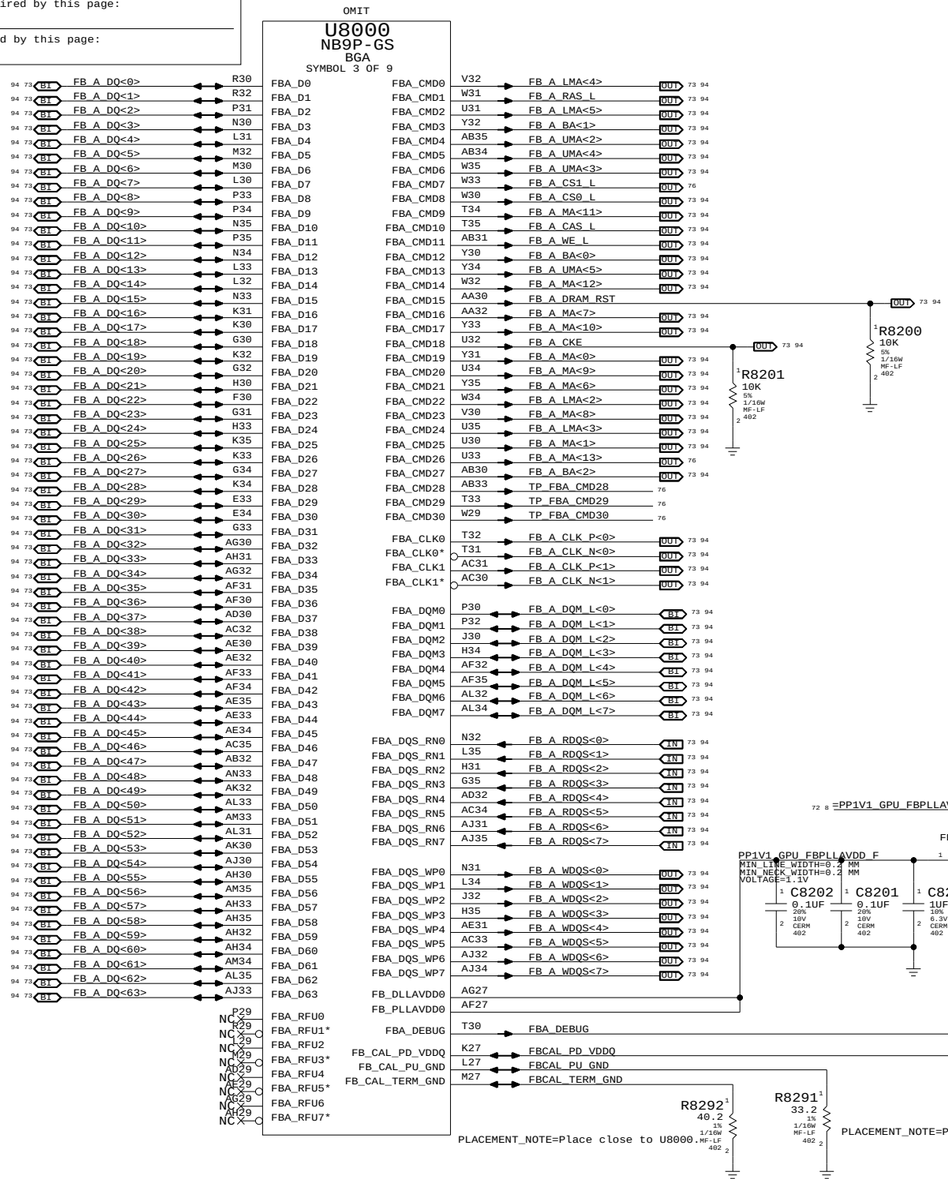
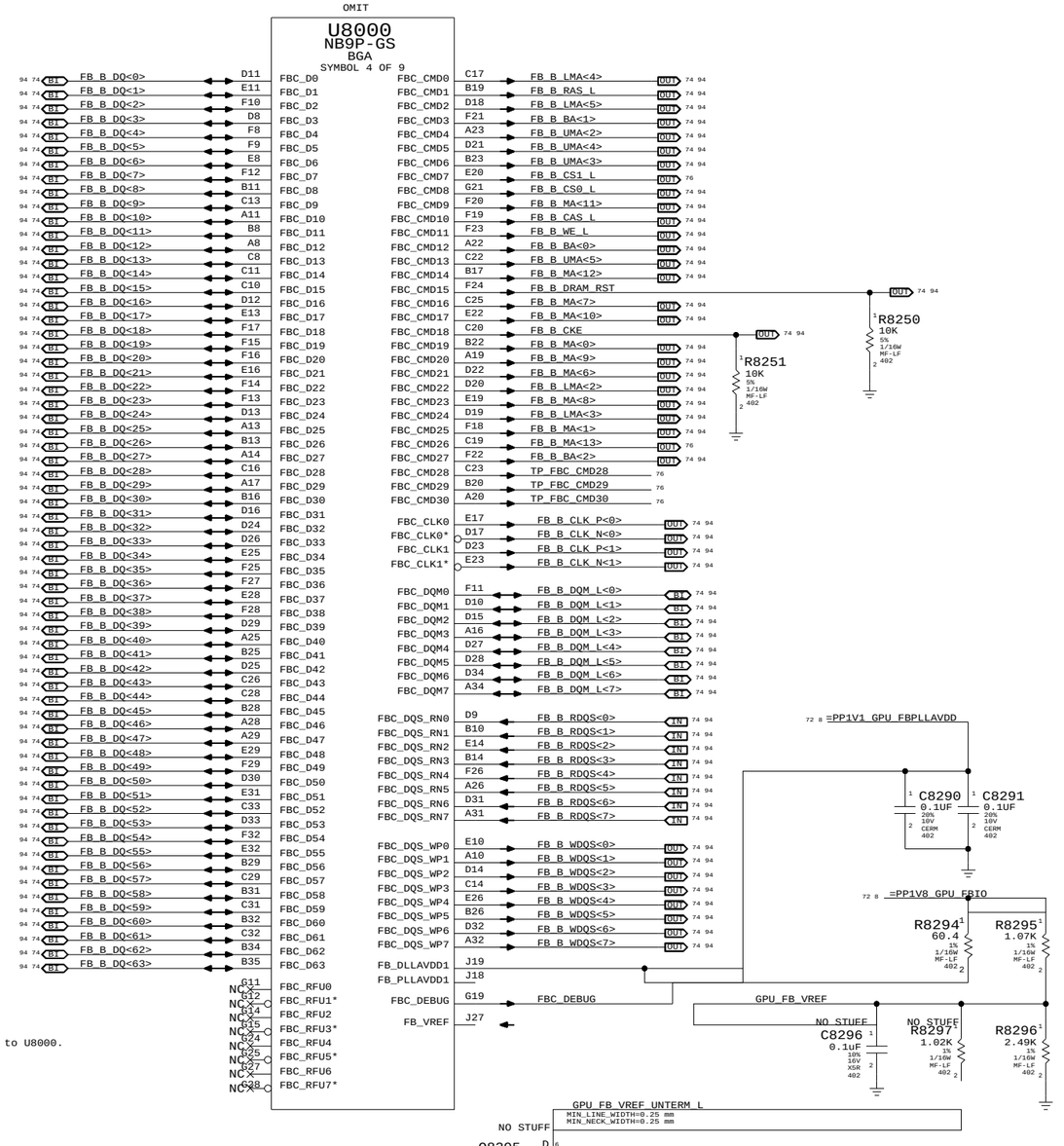
# Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)




## NV G96 Frame Buffer I/F

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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| SCALE | SHT | OF |
| NONE | 82 | 109 |

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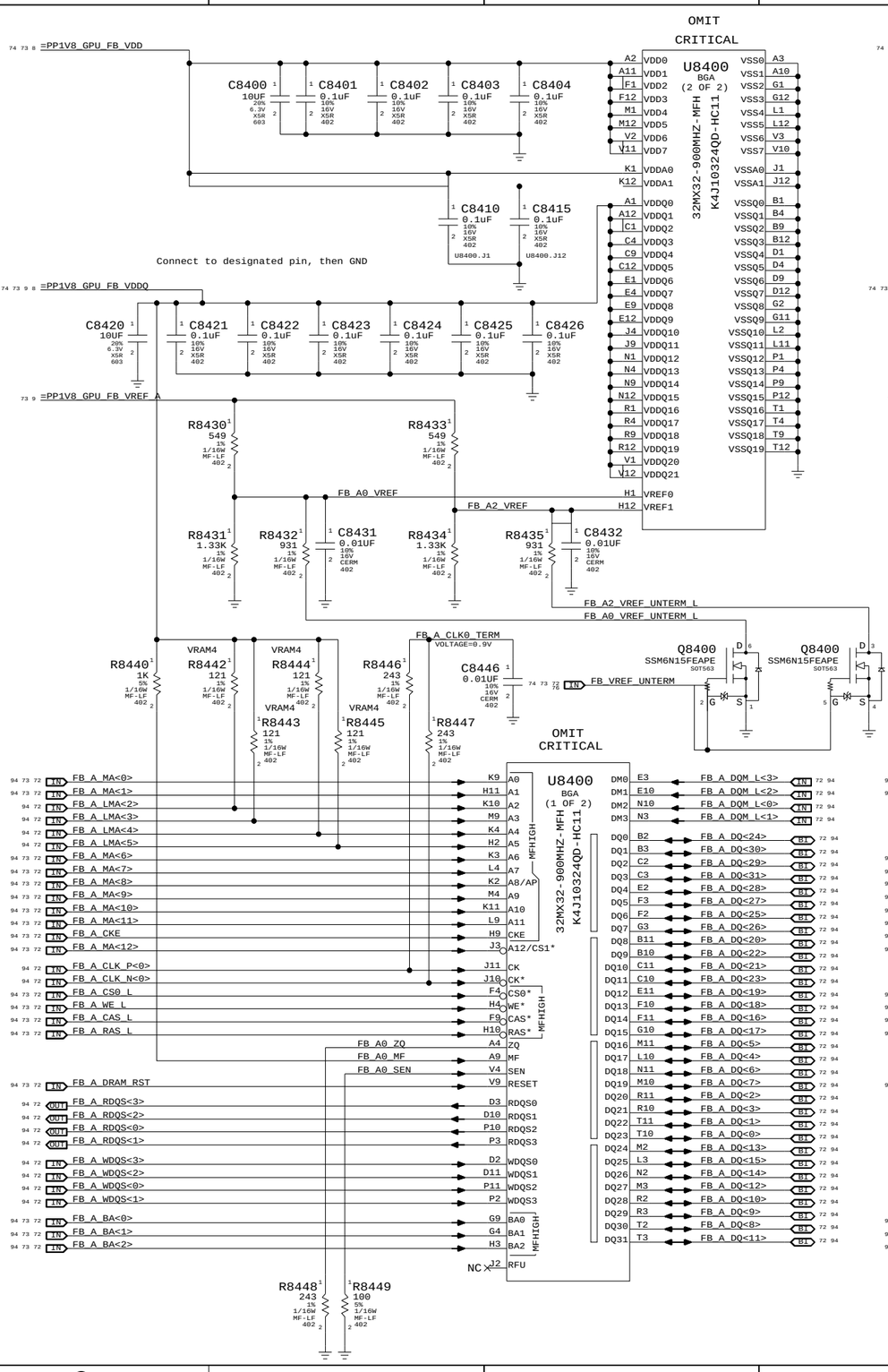


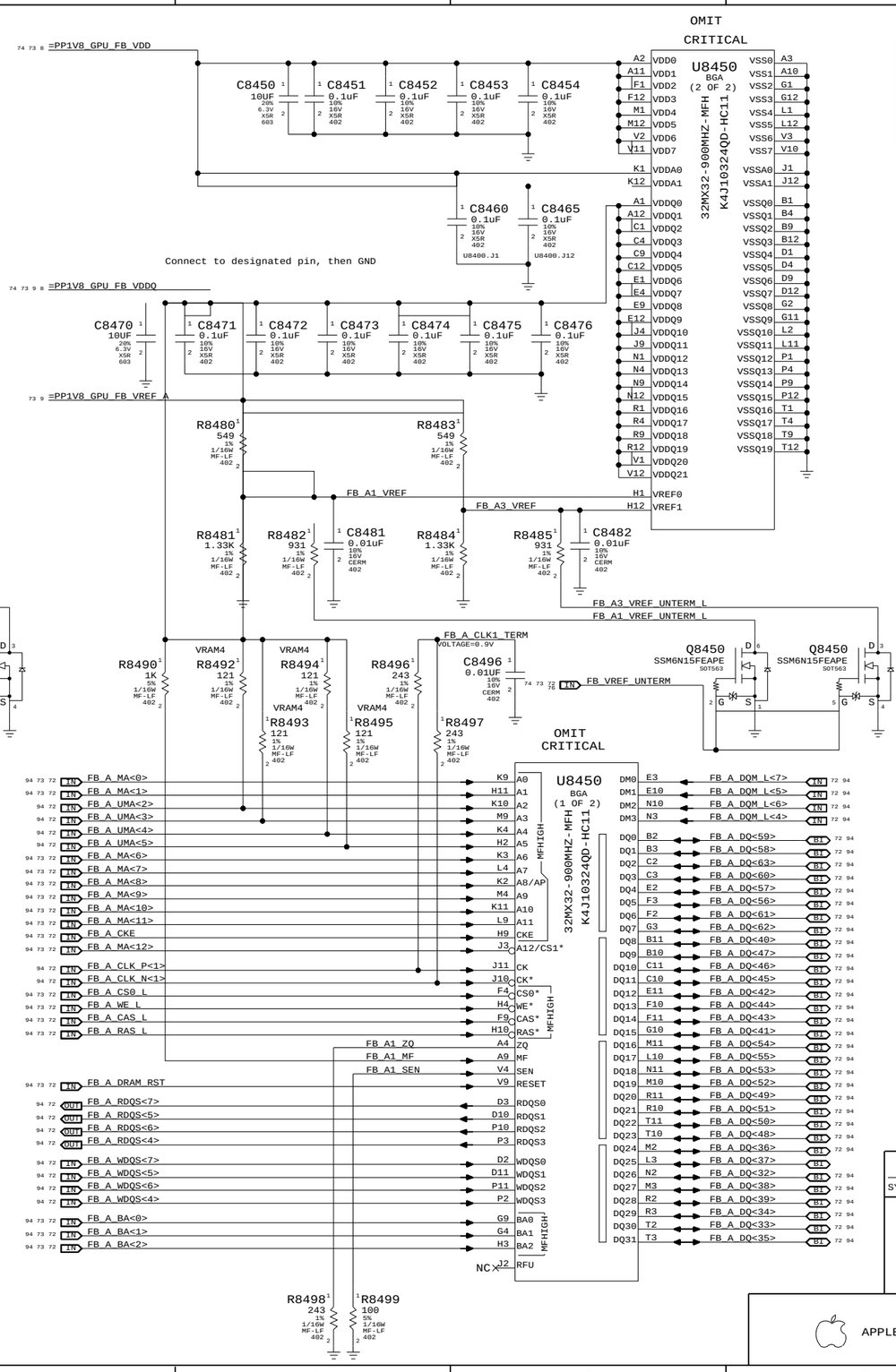


## Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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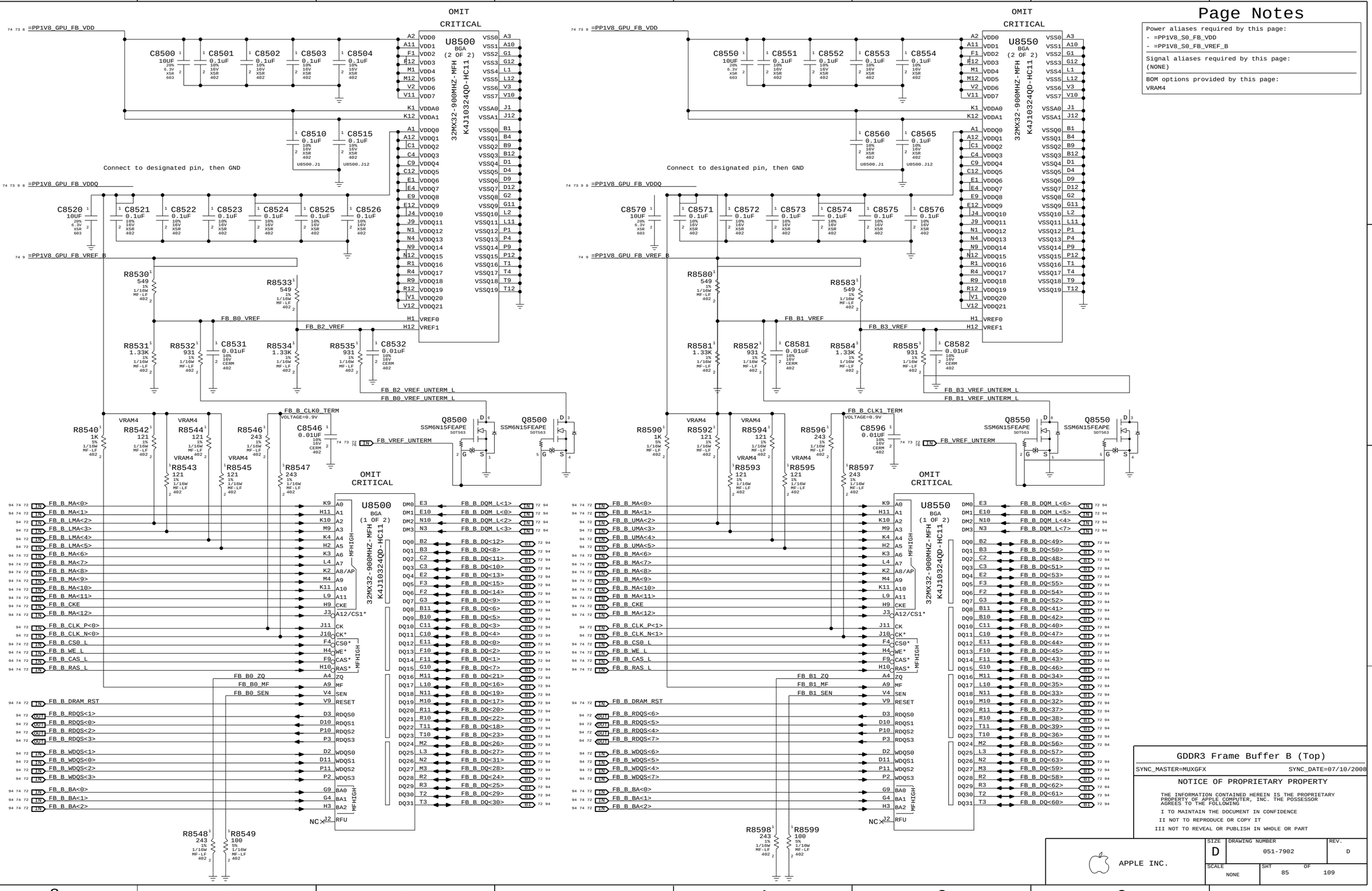


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# Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
=PP3V3_GPU_VDD33

OMIT
U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

J9 VDD33_1
J10 VDD33_2
J11 VDD33_3
J12 VDD33_4
J13 VDD33_5

=PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

J25 RFU0
J26 RFU1
AK14 RFU0_GND
K9 RFU1_GND

GPU_ROM_CS_L → C3 ROM_CS*
GPU_ROM_SCLK → D4 ROM_SCLK
GPU_ROM_SI → D3 ROM_SI
GPU_ROM_SO → C4 ROM_SO

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

GPU_STRAP_REF_3V3_PD → N9 STRAP_REF_3V3
GPU_STRAP_REF_MIOB_PD → M9 STRAP_REF_MIOB (1PD)

=PP3V3_GPU_MIO
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

=PP3V3_GPU_MIO
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1uF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD → AP35 TESTMODE
GPU_MIOA_VREF → N5 MIOA_VREF
GPU_MIOB_VREF → AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ → U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND → T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ → AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND → AA6 MIOB_CAL_PU_GND

=PP1V1_GPU_PLLVDD
L8630 FERR-220-OHM 0402
PP1V1_GPU_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

=PP1V1_GPU_H_PLLVDD
L8635 FERR-220-OHM 0402
PP1V1_GPU_H_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

=PP1V1_GPU_VID_PLLVDD
L8640 FERR-220-OHM 0402
PP1V1_GPU_VID_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

AF9 SP_PLLVDD
AE9 PLLVDD
AD9 VID_PLLVDD

GPU_XTALIN → B1 XTAL_IN
GPU_XTALOUT → B2 XTAL_OUT
GPU_XTALOUTBUFF → D1 XTAL_OUTBUFF
GPU_XTALSSIN → D2 XTAL_SSIN

| | | | |
|---|---|---|---|
| GPIO0 | K1 | GPU_GPIO_0 | B1 |
| GPIO1 | K2 | GPU_GPIO_1 | B1 |
| GPIO2 | K3 | GPU_GPIO_2 | B1 |
| GPIO3 | H3 | GPU_GPIO_3 | B1 |
| GPIO4 | H2 | GPU_GPIO_4 | B1 |
| GPIO5 | H1 | GPU_GPIO_5 | B1 |
| GPIO6 | H4 | GPU_GPIO_6 | B1 |
| GPIO7 | H5 | GPU_GPIO_7 | B1 |
| GPIO8 | H6 | GPU_GPIO_8 | B1 |
| GPIO9 | J7 | GPU_GPIO_9 | B1 |
| GPIO10 | K4 | GPU_GPIO_10 | B1 |
| GPIO11 | K5 | GPU_GPIO_11 | B1 |
| GPIO12 | H7 | GPU_GPIO_12 | B1 |
| GPIO13 | J4 | GPU_GPIO_13 | B1 |
| GPIO14 | J6 | GPU_GPIO_14 | B1 |
| GPIO15 | L1 | GPU_GPIO_15 | B1 |
| GPIO16 | L2 | GPU_GPIO_16 | B1 |
| GPIO17 | L4 | GPU_GPIO_17 | B1 |
| GPIO18 | M4 | GPU_GPIO_18 | B1 |
| GPIO19 | L7 | GPU_GPIO_19 | B1 |
| GPIO20 | L5 | GPU_GPIO_20 | B1 |
| GPIO21 | K6 | GPU_GPIO_21 | B1 |
| GPIO22 | L6 | GPU_GPIO_22 | B1 |
| GPIO23 | M6 | GPU_GPIO_23 | B1 |
| HDA_SDI | C7 | GPU_HDA_SDI | OUT |
| HDA_SDO | B7 | GPU_HDA_SDO | OUT |
| HDA_SYNC | A7 | GPU_HDA_SYNC | OUT |
| HDA_BCLK | D7 | GPU_HDA_BCLK | OUT |
| HDA_RST* | D6 | GPU_HDA_RST_L | OUT |
| SPDIF | A5 | GPU_SPDIF | IN |
| BUFRST* | A4 | TP_GPU_BUFRST_L | OUT |
| JTAG_TCK | AP14 | GPU_JTAG_TCK | IN |
| JTAG_TDI | AN14 | GPU_JTAG_TDI | IN |
| JTAG_TDO | AN16 | GPU_JTAG_TDO | OUT |
| JTAG_TMS | AR14 | GPU_JTAG_TMS | IN |
| JTAG_TRST* | AP16 | GPU_JTAG_TRST_L | IN |
| MIOA_CLKIN | N4 | GPU_MIOA_CLKIN | IN |
| MIOA_CLKOUT | R4 | GPU_MIOA_CLKOUT_P | B1 |
| MIOA_CLKOUT* | T4 | GPU_MIOA_CLKOUT_N | B1 |
| MIOA_CTL3 | P5 | GPU_MIOA_CTL3 | B1 |
| MIOA_DE | N2 | GPU_MIOA_DE | B1 |
| MIOA_D0 | N1 | GPU_MIOA_D<0> | B1 |
| MIOA_D1 | P4 | GPU_MIOA_D<1> | B1 |
| MIOA_D2 | P1 | GPU_MIOA_D<2> | B1 |
| MIOA_D3 | P2 | GPU_MIOA_D<3> | B1 |
| MIOA_D4 | P3 | GPU_MIOA_D<4> | B1 |
| MIOA_D5 | T3 | GPU_MIOA_D<5> | B1 |
| MIOA_D6 | T2 | GPU_MIOA_D<6> | B1 |
| MIOA_D7 | T1 | GPU_MIOA_D<7> | B1 |
| MIOA_D8 | U4 | GPU_MIOA_D<8> | B1 |
| MIOA_D9 | U1 | GPU_MIOA_D<9> | B1 |
| MIOA_D10 | U2 | GPU_MIOA_D<10> | B1 |
| MIOA_D11 | U3 | GPU_MIOA_D<11> | B1 |
| MIOA_D12 | R6 | GPU_MIOA_D<12> | B1 |
| MIOA_D13 | T6 | GPU_MIOA_D<13> | B1 |
| MIOA_D14 | N6 | GPU_MIOA_D<14> | B1 |
| MIOA_HSYNC | N3 | GPU_MIOA_HSYNC | B1 |
| MIOA_VSYNC | L3 | GPU_MIOA_VSYNC | B1 |
| MIOB_CLKIN | AE1 | GPU_MIOB_CLKIN | IN |
| MIOB_CLKOUT | V4 | GPU_MIOB_CLKOUT_P | B1 |
| MIOB_CLKOUT* | W4 | GPU_MIOB_CLKOUT_N | B1 |
| MIOB_CTL3 | W3 | GPU_MIOB_CTL3 | B1 |
| MIOB_DE | Y5 | GPU_MIOB_DE | B1 |
| MIOB_D0 | Y1 | GPU_MIOB_D<0> | B1 |
| MIOB_D1 | Y2 | GPU_MIOB_D<1> | B1 |
| MIOB_D2 | Y3 | GPU_MIOB_D<2> | B1 |
| MIOB_D3 | AB3 | GPU_MIOB_D<3> | B1 |
| MIOB_D4 | AB2 | GPU_MIOB_D<4> | B1 |
| MIOB_D5 | AB1 | GPU_MIOB_D<5> | B1 |
| MIOB_D6 | AC4 | GPU_MIOB_D<6> | B1 |
| MIOB_D7 | AC1 | GPU_MIOB_D<7> | B1 |
| MIOB_D8 | AC2 | GPU_MIOB_D<8> | B1 |
| MIOB_D9 | AC3 | GPU_MIOB_D<9> | B1 |
| MIOB_D10 | AE3 | GPU_MIOB_D<10> | B1 |
| MIOB_D11 | AE2 | GPU_MIOB_D<11> | B1 |
| MIOB_D12 | U6 | GPU_MIOB_D<12> | B1 |
| MIOB_D13 | W6 | GPU_MIOB_D<13> | B1 |
| MIOB_D14 | Y6 | GPU_MIOB_D<14> | B1 |
| MIOB_D15 | W5 | GPU_STRAP<0> | B1 |
| MIOB_D16 | W7 | GPU_STRAP<1> | B1 |
| MIOB_D17 | V7 | GPU_STRAP<2> | B1 |
| MIOB_HSYNC | W1 | GPU_MIOB_HSYNC | B1 |
| MIOB_VSYNC | W2 | GPU_MIOB_VSYNC | B1 |
| THERMDP | B5 | GPU_THERMD_P | IN |
| THERMDN | B4 | GPU_THERMD_N | OUT |
| PGOOD_OUT* | C5 | TP_GPU_PGOOD_OUT_L | OUT |

## NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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| SCALE: NONE | SHT 86 OF 109 | |

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## GPIOs

| | Native Func | | |
|---|---|---|---|
| GPU_GPIO_0 | GP | NC_GPU_GPIO_0 | MAKE_BASE=TRUE |
| GPU_GPIO_1 | HPDC | DP_EG_HPD | IN 80 |
| GPU_GPIO_2 | LCD0_BL_PWM | TP_LVDS_EG_BKL_PWM | MAKE_BASE=TRUE |
| GPU_GPIO_3 | LCD0_VDD | EG_LCD_PWR_EN | MAKE_BASE=TRUE; 76 83 |
| GPU_GPIO_4 | LCD0_BL_EN | EG_BKLT_EN | MAKE_BASE=TRUE; 76 83 |
| GPU_GPIO_5 | VID0 | TP_GPU_GSTATE<0> | MAKE_BASE=TRUE |
| GPU_GPIO_6 | VID1 | TP_GPU_GSTATE<1> | MAKE_BASE=TRUE |
| GPU_GPIO_7 | VID2/MEM_VID | GPIO7_FBVDD_ALTVO | MAKE_BASE=TRUE; 76 82 |
| GPU_GPIO_8 | THERM | SMC_GFX_OVERTEMP_R_L | MAKE_BASE=TRUE; 76 |
| GPU_GPIO_9 | FAN_PWM | SMC_GFX_THROTTLE_R_L | MAKE_BASE=TRUE; 76 |
| GPU_GPIO_10 | MEM_VREF | FB_VREF_UNTERM | MAKE_BASE=TRUE; 72 73 74 76 |
| GPU_GPIO_11 | SLI_SYNC | GPU_VCORE_VID0 | MAKE_BASE=TRUE; OUT 78 |
| GPU_GPIO_12 | AC_DET | GPU_VCORE_VID1 | MAKE_BASE=TRUE; OUT 78 |
| GPU_GPIO_13 | PWR_CTL0 | GPU_VCORE_VID2 | MAKE_BASE=TRUE; OUT 78 |
| GPU_GPIO_14 | PWR_CTL1 | TP_GPU_VCORE_VID3 | MAKE_BASE=TRUE |

## GPIOs

| | Native Func | | |
|---|---|---|---|
| GPU_GPIO_15 | HPDE | NC_GPU_GPIO_15 | MAKE_BASE=TRUE |
| GPU_GPIO_16 | DVI_MODE0 | EG_DP_CA_DET | 76 |
| GPU_GPIO_17 | HDMI_DETECT0 | NC_GPU_GPIO_17 | MAKE_BASE=TRUE |
| GPU_GPIO_18 | DVI_MODE1 | NC_GPU_GPIO_18 | MAKE_BASE=TRUE |
| GPU_GPIO_19 | HDMI_DETECT1 | NC_GPU_GPIO_19 | MAKE_BASE=TRUE |
| GPU_GPIO_20 | HPDD | NC_GPU_GPIO_20 | MAKE_BASE=TRUE |
| GPU_GPIO_21 | HPDF | NC_GPU_GPIO_21 | MAKE_BASE=TRUE |
| GPU_GPIO_22 | SWAPRDY_A | NC_GPU_GPIO_22 | MAKE_BASE=TRUE |
| GPU_GPIO_23 | GP | NC_GPU_GPIO_23 | MAKE_BASE=TRUE NO_TEST=TRUE |

## Renamed signals

| | | |
|---|---|---|
| GPU_XTALOUT | MAKE_BASE=TRUE | GPU_XTALOUT |
| GPU_CLK27M | MAKE_BASE=TRUE | GPU_XTALIN |
| GPU_CLK27M_SS | MAKE_BASE=TRUE | GPU_XTALSSIN |
| GPU_TDIODE_P | MAKE_BASE=TRUE | GPU_THERMD_P |
| GPU_TDIODE_N | MAKE_BASE=TRUE | GPU_THERMD_N |
| LVDS_EG_DDC_CLK | MAKE_BASE=TRUE | GPU_I2CA_SCL |
| LVDS_EG_DDC_DATA | MAKE_BASE=TRUE | GPU_I2CA_SDA |
| DP_EG_DDC_CLK | MAKE_BASE=TRUE | GPU_I2CB_SCL |
| DP_EG_DDC_DATA | MAKE_BASE=TRUE | GPU_I2CB_SDA |

## Unused signals

| | | |
|---|---|---|
| NC_GPU_SPDIF | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_SPDIF |
| NC_CPU_HDA_SDI | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_HDA_SDI |
| NC_CPU_HDA_SD0 | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_HDA_SDO |
| NC_CPU_HDA_SYNC | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_HDA_SYNC |
| NC_CPU_HDA_BCLK | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_HDA_BCLK |
| NC_CPU_HDA_RST_L | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_HDA_RST_L |
| NC_FBA_MA<13> | MAKE_BASE=TRUE NO_TEST=TRUE | FB_A_MA<13> |
| NC_FBB_MA<13> | MAKE_BASE=TRUE NO_TEST=TRUE | FB_B_MA<13> |
| NC_FBA_CMD28 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBA_CMD28 |
| NC_FBC_CMD28 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBC_CMD28 |
| NC_FBA_CMD29 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBA_CMD29 |
| NC_FBC_CMD29 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBC_CMD29 |
| NC_FBA_CMD30 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBA_CMD30 |
| NC_FBC_CMD30 | MAKE_BASE=TRUE NO_TEST=TRUE | TP_FBC_CMD30 |
| NC_GPU_ROM_CS_L | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_ROM_CS_L |
| NC_FB_A_CS1_L | MAKE_BASE=TRUE NO_TEST=TRUE | FB_A_CS1_L |
| NC_FB_B_CS1_L | MAKE_BASE=TRUE NO_TEST=TRUE | FB_B_CS1_L |

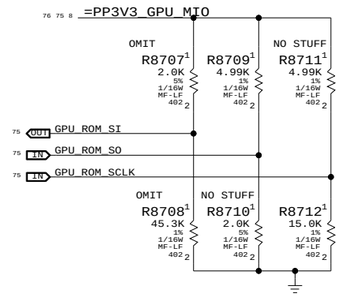
## Unused I2C Buses

| | | |
|---|---|---|
| NC_GPU_I2CC_SCL | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CC_SCL |
| NC_GPU_I2CC_SDA | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CC_SDA |
| NC_GPU_I2CD_SCL | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CD_SCL |
| NC_GPU_I2CD_SDA | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CD_SDA |
| NC_GPU_I2CE_SCL | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CE_SCL |
| NC_GPU_I2CE_SDA | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CE_SDA |
| NC_GPU_I2CH_SCL | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CH_SDA |
| NC_GPU_I2CH_SDA | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_I2CH_SCL |

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

| | | |
|---|---|---|
| TP_LVDS_EG_B_CLK_P | MAKE_BASE=TRUE | LVDS_EG_B_CLK_P |
| TP_LVDS_EG_B_CLK_N | MAKE_BASE=TRUE | LVDS_EG_B_CLK_N |
| NC_LVDS_EG_A_DATA_P<3> | MAKE_BASE=TRUE NO_TEST=TRUE | LVDS_EG_A_DATA_P<3> |
| NC_LVDS_EG_A_DATA_N<3> | MAKE_BASE=TRUE NO_TEST=TRUE | LVDS_EG_A_DATA_N<3> |
| NC_LVDS_EG_B_DATA_P<3> | MAKE_BASE=TRUE NO_TEST=TRUE | LVDS_EG_B_DATA_P<3> |
| NC_LVDS_EG_B_DATA_N<3> | MAKE_BASE=TRUE NO_TEST=TRUE | LVDS_EG_B_DATA_N<3> |

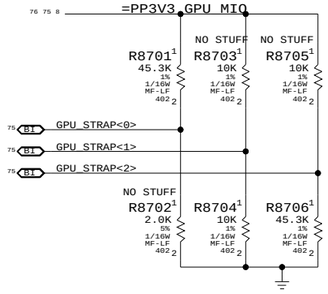
## Config Straps



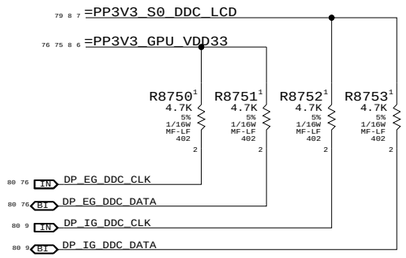

| Physical Strapping Pin | Strapping Bit 3 | Strapping Bit 2 | Strapping Bit 1 | Strapping Bit 0 |
|---|---|---|---|---|
| ROM_SO | XCLK_277 | TVMODE[2] | TVMODE[1] | TVMODE[0] |
| ROM_SCLK | PCI_DEVID[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLLEN_TERM100 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] |
| STRAP 2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP 1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP 0 | USER[3] | USER[2] | USER[1] | USER[0] |

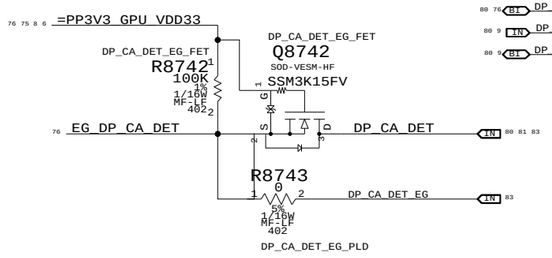
| Strap S1/S2 Bit[3:0] | PU/PD | Rval |
|---|---|---|
| 0 0000 | PD | 5k |
| 1 0001 | PD | 10k |
| 2 0010 | PD | 15k |
| 3 0011 | PD | 20k |
| 4 0100 | PD | 25k |
| 5 0101 | PD | 30k |
| 6 0110 | PD | 35k |
| 7 0111 | PD | 45k |

| Strap S1/S2 Bit[3:0] | PU/PD | Rval |
|---|---|---|
| 8 1000 | PU | 5k |
| 9 1001 | PU | 10k |
| A 1010 | PU | 15k |
| B 1011 | PU | 20k |
| C 1100 | PU | 25k |
| D 1101 | PU | 30k |
| E 1110 | PU | 35k |
| F 1111 | PU | 45k |




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0378 | 1 | RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF | R8708 | | VRAM_512_SAMSUNG |
| 114S0368 | 1 | RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF | R8708 | | VRAM_512_HYNIX |
| 114S0361 | 1 | RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF | R8708 | | VRAM_512_QIMONDA |
| 114S0343 | 1 | RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF | R8708 | | VRAM_256_SAMSUNG |
| 114S0331 | 1 | RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF | R8708 | | VRAM_256_HYNIX |
| 114S0378 | 1 | RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF | R8707 | | VRAM_1024_SAMSUNG |
| 114S0361 | 1 | RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF | R8707 | | VRAM_1024_QIMONDA |

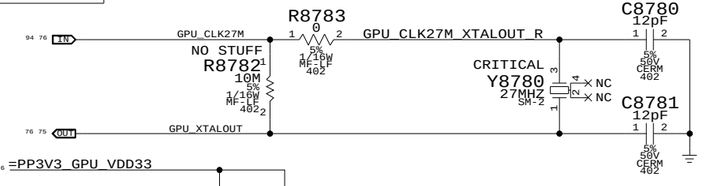



## Isolation FETs for DP MUX inputs

G96 HDCP ROM APN is 341S2272, blank device is 335S0574.

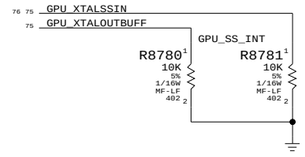
## GPU 27MHz Crystal




G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

| | | |
|---|---|---|
| NC_GPU_MIOA_CLKOUT_P | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_CLKOUT_P |
| NC_GPU_MIOA_CLKOUT_N | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_CLKOUT_N |
| NC_GPU_MIOA_CTL3 | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_CTL3 |
| TP_GPU_MIOA_DE | MAKE_BASE=TRUE | GPU_MIOA_DE |
| TP_GPU_MIOA_D<9..0> | MAKE_BASE=TRUE | GPU_MIOA_D<9..0> |
| NC_GPU_MIOA_CLKIN | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_CLKIN |
| NC_GPU_MIOA_D<14..10> | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_D<14..10> |
| NC_GPU_MIOA_HSYNC | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_HSYNC |
| NC_GPU_MIOA_VSYNC | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOA_VSYNC |
| NC_GPU_MIOB_CLKIN | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_CLKIN |
| NC_GPU_MIOB_CLKOUT_P | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_CLKOUT_P |
| NC_GPU_MIOB_CLKOUT_N | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_CLKOUT_N |
| NC_GPU_MIOB_CTL3 | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_CTL3 |
| NC_GPU_MIOB_DE | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_DE |
| NC_GPU_MIOB_D<14..0> | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_D<14..0> |
| NC_GPU_MIOB_VSYNC | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_VSYNC |
| NC_GPU_MIOB_HSYNC | MAKE_BASE=TRUE NO_TEST=TRUE | GPU_MIOB_HSYNC |

## Unused Clocks




## G96 GPIOs & Straps

SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008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|---|---|---|
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| SCALE: NONE | SHT 87 OF 109 | |

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# Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

8 =PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10
PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8810 FERR-220-OHM 0402
8 =PP1V1_GPU_IFPCD_IOVDD
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F 77
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V
I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPCD_PLLVDD_F 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

GPU_IFPEF_RSET 77
GPU_IFPCD_RSET 77
GPU_IFPAB_RSET 77
R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

PP1V1_GPU_IFPEF_IOVDD_F 77
PP1V8_GPU_IFPEF_PLLVDD_F 77
Power inputs must be pulled down if not used
R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

| | | | |
|---|---|---|---|
| AG9 | IFPA_IOVDD | | |
| AG10 | IFPB_IOVDD | | |
| AJ8 | IFPC_IOVDD | | |
| AK8 | IFPD_IOVDD | | |
| AE7 | IFPE_IOVDD | | |
| AD7 | IFPF_IOVDD | | |
| AK9 | IFPAB_PLLVDD | | |
| AJ11 | IFPAB_RSET | | |
| AJ9 | IFPCD_PLLVDD | | |
| AK7 | IFPCD_RSET | | |
| AJ6 | IFPEF_PLLVDD | | |
| AL1 | IFPEF_RSET | | |
| G1 | I2CA_SCL | | |
| G4 | I2CA_SDA | | |
| E3 | I2CC_SCL | | |
| E4 | I2CC_SDA | | |
| E2 | I2CS_SCL | | |
| E1 | I2CS_SDA | | |
| F6 | I2CH_SCL | | |
| G6 | I2CH_SDA | | |
| G3 | I2CB_SCL | | |
| G2 | I2CB_SDA | | |
| F4 | I2CD_SCL | | |
| G5 | I2CD_SDA | | |
| D5 | I2CE_SCL | | |
| E5 | I2CE_SDA | | |
| AM11 | IFPA_TXC | LVDS_EG_A_CLK_P | OUT 83 94 |
| AM12 | IFPA_TXC* | LVDS_EG_A_CLK_N | OUT 83 94 |
| AM8 | IFPA_TXD0 | LVDS_EG_A_DATA_P<0> | OUT 83 94 |
| AL8 | IFPA_TXD0* | LVDS_EG_A_DATA_N<0> | OUT 83 94 |
| AM10 | IFPA_TXD1 | LVDS_EG_A_DATA_P<1> | OUT 83 94 |
| AM9 | IFPA_TXD1* | LVDS_EG_A_DATA_N<1> | OUT 83 94 |
| AK10 | IFPA_TXD2 | LVDS_EG_A_DATA_P<2> | OUT 83 94 |
| AL10 | IFPA_TXD2* | LVDS_EG_A_DATA_N<2> | OUT 83 94 |
| AK11 | IFPA_TXD3 | LVDS_EG_A_DATA_P<3> | OUT 76 |
| AL11 | IFPA_TXD3* | LVDS_EG_A_DATA_N<3> | OUT 76 |
| AP13 | IFPB_TXC | LVDS_EG_B_CLK_P | OUT 76 |
| AN13 | IFPB_TXC* | LVDS_EG_B_CLK_N | OUT 76 |
| AN8 | IFPB_TXD4 | LVDS_EG_B_DATA_P<0> | OUT 83 94 |
| AP8 | IFPB_TXD4* | LVDS_EG_B_DATA_N<0> | OUT 83 94 |
| AP10 | IFPB_TXD5 | LVDS_EG_B_DATA_P<1> | OUT 83 94 |
| AN10 | IFPB_TXD5* | LVDS_EG_B_DATA_N<1> | OUT 83 94 |
| AR11 | IFPB_TXD6 | LVDS_EG_B_DATA_P<2> | OUT 83 94 |
| AR10 | IFPB_TXD6* | LVDS_EG_B_DATA_N<2> | OUT 83 94 |
| AN11 | IFPB_TXD7 | LVDS_EG_B_DATA_P<3> | OUT 76 |
| AP11 | IFPB_TXD7* | LVDS_EG_B_DATA_N<3> | OUT 76 |
| AP2 | IFPC_AUX | DP_EG_AUX_CH_P | OUT 80 94 |
| AN3 | IFPC_AUX* | DP_EG_AUX_CH_N | OUT 80 94 |
| AM7 | IFPC_L0 | DP_EG_ML_P<0> | OUT 80 94 |
| AM6 | IFPC_L0* | DP_EG_ML_N<0> | OUT 80 94 |
| AL5 | IFPC_L1 | DP_EG_ML_P<1> | OUT 80 94 |
| AM5 | IFPC_L1* | DP_EG_ML_N<1> | OUT 80 94 |
| AM3 | IFPC_L2 | DP_EG_ML_P<2> | OUT 80 94 |
| AM4 | IFPC_L2* | DP_EG_ML_N<2> | OUT 80 94 |
| AP1 | IFPC_L3 | DP_EG_ML_P<3> | OUT 80 94 |
| AR2 | IFPC_L3* | DP_EG_ML_N<3> | OUT 80 94 |
| AP4 | IFPD_AUX | NC | |
| AN4 | IFPD_AUX* | NC | |
| AR8 | IFPD_L0 | NC | |
| AR7 | IFPD_L0* | NC | |
| AF7 | IFPD_L1 | NC | |
| AN7 | IFPD_L1* | NC | |
| AN5 | IFPD_L2 | NC | |
| AP5 | IFPD_L2* | NC | |
| AR5 | IFPD_L3 | NC | |
| AR4 | IFPD_L3* | NC | |
| AE4 | IFPE_AUX | NC | |
| AD4 | IFPE_AUX* | NC | |
| AH6 | IFPE_L0 | NC | |
| AH5 | IFPE_L0* | NC | |
| AH4 | IFPE_L1 | NC | |
| AG4 | IFPE_L1* | NC | |
| AF4 | IFPE_L2 | NC | |
| AE5 | IFPE_L2* | NC | |
| AE6 | IFPE_L3 | NC | |
| AE7 | IFPE_L3* | NC | |
| AF3 | IFPF_AUX | NC | |
| AF2 | IFPF_AUX* | NC | |
| AL2 | IFPF_L0 | NC | |
| AL3 | IFPF_L0* | NC | |
| AJ3 | IFPF_L1 | NC | |
| AJ2 | IFPF_L1* | NC | |
| AJ1 | IFPF_L2 | NC | |
| AH1 | IFPF_L2* | NC | |
| AH2 | IFPF_L3 | NC | |
| AH3 | IFPF_L3* | NC | |
| AJ12 | DACA_VDD | | |
| AK12 | DACA_VREF | | |
| AK13 | DACA_RSET | | |
| AC6 | DACB_VDD | | |
| AC5 | DACB_VREF | | |
| AB6 | DACB_RSET | | |
| AG7 | DACC_VDD | | |
| AK6 | DACC_VREF | | |
| AK7 | DACC_RSET | | |
| AM15 | DACA_RED | NC | |
| AM14 | DACA_GREEN | NC | |
| AL14 | DACA_BLUE | NC | |
| AM13 | DACA_HSYNC | NC | |
| AL13 | DACA_VSYNC | NC | |
| AA4 | DACB_RED | NC | |
| AA3 | DACB_GREEN | NC | |
| Y4 | DACB_BLUE | NC | |
| AB5 | DACB_CSYNC | NC | |
| AK4 | DACC_RED | NC | |
| AL4 | DACC_GREEN | NC | |
| AJ4 | DACC_BLUE | NC | |
| AM1 | DACC_HSYNC | NC | |
| AM2 | DACC_VSYNC | NC | |

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD
R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402
NO STUFF

NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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# GPU VCore Regulator

=PP5V_S3_GPUVCORE
R8911 1 1/10W MF-LF 402
PP5V_S5_GFXIMVP6_PVCC
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
C8902 4.7UF 20% 6.3V X5R-CERM 402
C8903 0.01UF 10% 16V X7R-CERM 402
R8904 10 1% 1/10W MF-LF 402
PP5V_S5_GFXIMVP6_VDD
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
C8901 1UF 10% 16V X5R 402
R8905 150K 1% 1/16W MF-LF 402
GFXIMVP6_RBIAS
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
C8904 0.033UF 10% 16V X5R 402
GFXIMVP6_SOFT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_IMON
=PP3V3_GPU_VCORELOGIC
R8907 10K 1% 1/10W MF-LF 402
R8910 10K 1% 1/10W MF-LF 402
GPUVCORE_PGOOD
GFXIMVP6_VID0
GFXIMVP6_VID1
GFXIMVP6_VID2
GFXIMVP6_VID3
GFXIMVP6_VID4
=GPUVCORE_EN
GFXIMVP6_AF_EN
GFXIMVP6_FDE
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_VSEN_P
GFXIMVP6_VSEN_N
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.3MM
C8923 0.001UF 10% 16V X5R 402
C8921 0.001UF 10% 16V CERM 402
(GFXIMVP6_AGND)
GPU_VDD_SENSE
MIN_NECK_WIDTH=0.20 mm MIN_LINE_WIDTH=0.25 mm VOLTAGE=1.25V
R8920 20 1% 1/10W MF-LF 402
C8920 0.001UF 10% 16V X5R 402
GPU_GND_SENSE
MIN_NECK_WIDTH=0.20 mm MIN_LINE_WIDTH=0.25 mm VOLTAGE=0V
R8908 20 1% 1/10W MF-LF 402
GFXIMVP6_VW
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
R8909 4.99K 1% 1/10W MF-LF 402
C8922 0.001UF 10% 16V X7R 402
PLACEMENT_NOTE=Place R8920 at U8900
PLACEMENT_NOTE=Place R8908 at U8900
C8950 180PF 5% 50V CERM 402
GFXIMVP6_COMP_RC
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.3MM
GFXIMVP6_COMP
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
R8950 374K 1% 1/16W MF-LF 402
C8952 68PF 5% 50V CERM 402-1
GFXIMVP6_FB
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
R8951 4.99K 1% 1/16W MF-LF 402
R8953 2.21K 1% 1/16W MF-LF 402
C8951 560PF 10% 50V CERM 402
GFXIMVP6_VDIFF_RC
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.3MM
GFXIMVP6_VDIFF
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

U8900 QFN ISL6263C
VDD PVCC RBIAS UGATE BOOT PHASE LGATE SOFT IMON PGOOD VID0 VID1 VID2 VID3 VID4 VR_ON AF_EN FDE VSEN RTN VW COMP FB VDIFF ICOMP PGND VSS THRM_PAD VIN VO OCSET ISP ISN DROOP

CRITICAL C8931 22UF 20% 25V POLY-TANT CASE-D2-SM
CRITICAL C8930 22UF 20% 25V POLY-TANT CASE-D2-SM
C8932 1UF 10% 25V X5R 603-1
C8933 1UF 10% 25V X5R 603-1
C8934 0.001UF 10% 50V X7R 402
=PPVIN_GPU_GPUVCORE
R8930 1K 5% 1/10W MF-LF 402
CRITICAL Q8950 RJK0305DPB LFPAK-HF
GFXIMVP6_VIN
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_UGATE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_BOOT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
C8956 0.22UF 10% 16V X7R 603
GFXIMVP6_PHASE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM SWITCH_NODE=TRUE
CRITICAL L8920 0.60UH-24A MPC0750LR60-SM
PPVCORE_GPU_REG_R
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CRITICAL Q8951 RJK0328DPB LFPAK-HF
GFXIMVP6_LGATE
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C8953 680pF 10% 50V X7R 402
R8940 0.001 1% 1W MF 1206
PPVCORE_GPU_REG
C8969 0.001UF 10% 50V X7R 402
C8968 10UF 20% 6.3V X5R 603
C8967 10UF 20% 6.3V X5R 603
C8966 10UF 20% 6.3V X5R 603
C8965 10UF 20% 6.3V X5R 603
CRITICAL C8942 330UF 20% 2.0V POLY-TANT D2T-SM2
CRITICAL C8943 330UF 20% 2.0V POLY-TANT D2T-SM2
Vout = 1.05V - 0.96V
25A max output (L8920 limit)
GFXIMVP6_PHASE_VSUM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.3MM
R8903 1K 1% 1/10W MF-LF 402
R8900 5.90K 1% 1/10W MF-LF 402
GFXIMVP6_VO
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_OCSET
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
GFXIMVP6_VSUM
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
C8906 330PF 5% 50V C0G 402
GFXIMVP6_DFB
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
R8902 9.76K 1% 1/16W MF-LF 402
C8971 68PF 5% 50V CERM 402-1
R8901 5.11K 1% 1/16W MF-LF 402
C8972 0.1UF 10% 16V X5R 402
GFXIMVP6_DROOP
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
(PPVCORE_GPU_REG)
GND_GFXIMVP6_AGND
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
XW8900 SM

=PP3V3_GPU_VCORELOGIC
GPU_VCORE_VID0
GPU_VCORE_VID1
GPU_VCORE_VID2
R8986 0 5% 1/16W MF-LF 402
R8990 0 5% 1/16W MF-LF 402
R8994 0 5% 1/16W MF-LF 402
GPUVID0_1 R8987 2.2K 5% 1/16W MF-LF 402
GPUVID1_1 R8984 2.2K 5% 1/16W MF-LF 402
GPUVID2_1 R8982 2.2K 5% 1/16W MF-LF 402
R8980 0 5% 1/16W MF-LF 402
GPUVID1_0 R8985 2.2K 5% 1/16W MF-LF 402
GPUVID2_0 R8983 2.2K 5% 1/16W MF-LF 402
R8988 0 5% 1/16W MF-LF 402
GFXIMVP6_VID0
GFXIMVP6_VID1
GFXIMVP6_VID2
GFXIMVP6_VID3
GFXIMVP6_VID4

## GPU VCore Setpoints

| VID3 | VID2 | VID1 | VID0 | Voltage | Max Batt | Balanced | Max perf |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0.90125V | M98 | | - |
| 1 | 1 | 1 | 0 | 0.92700V | - | M98 | - |
| 1 | 0 | 1 | 1 | 1.00425V | - | - | M98 |

Other VID states may not be valid

## M98 Default Vcore Setpoints

| BOM GROUP | BOM OPTIONS |
|---|---|
| GPUVID_0P90V | GPUVID2_1,GPUVID1_1,GPUVID0_1 |
| GPUVID_1P00V | GPUVID2_0,GPUVID1_1,GPUVID0_1 |

## GPU (G84M) Core Supply

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 89 OF 109 | |

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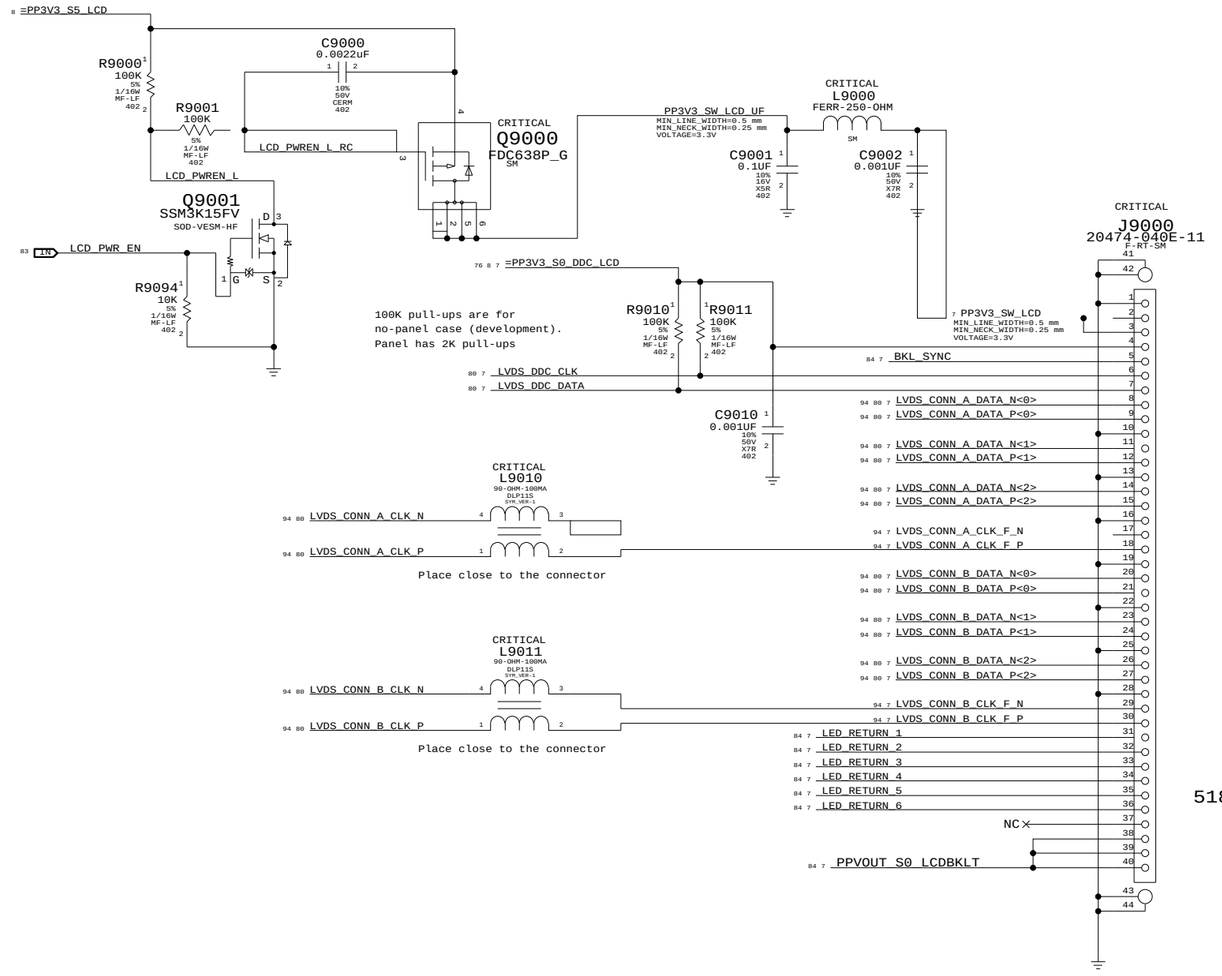
# LCD (LVDS) INTERFACE




518S0651

LVDS Display Connector

SYNC_MASTER=MUXGFX SYNC_DATE=02/25/2008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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 90 OF 109 | |

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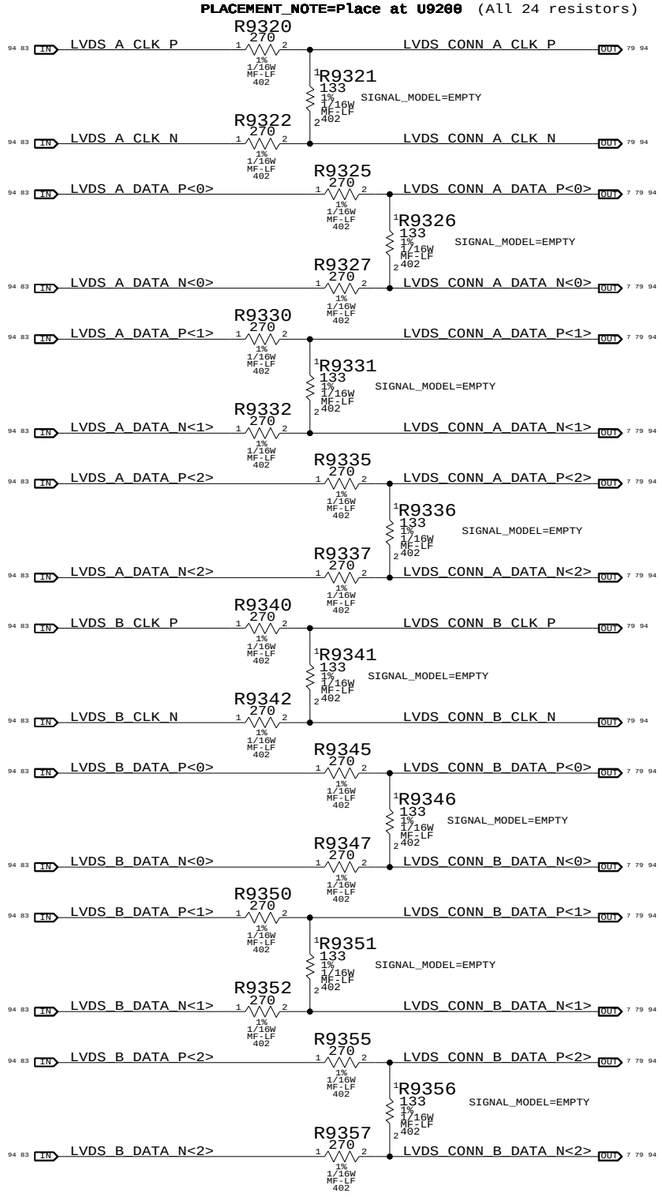
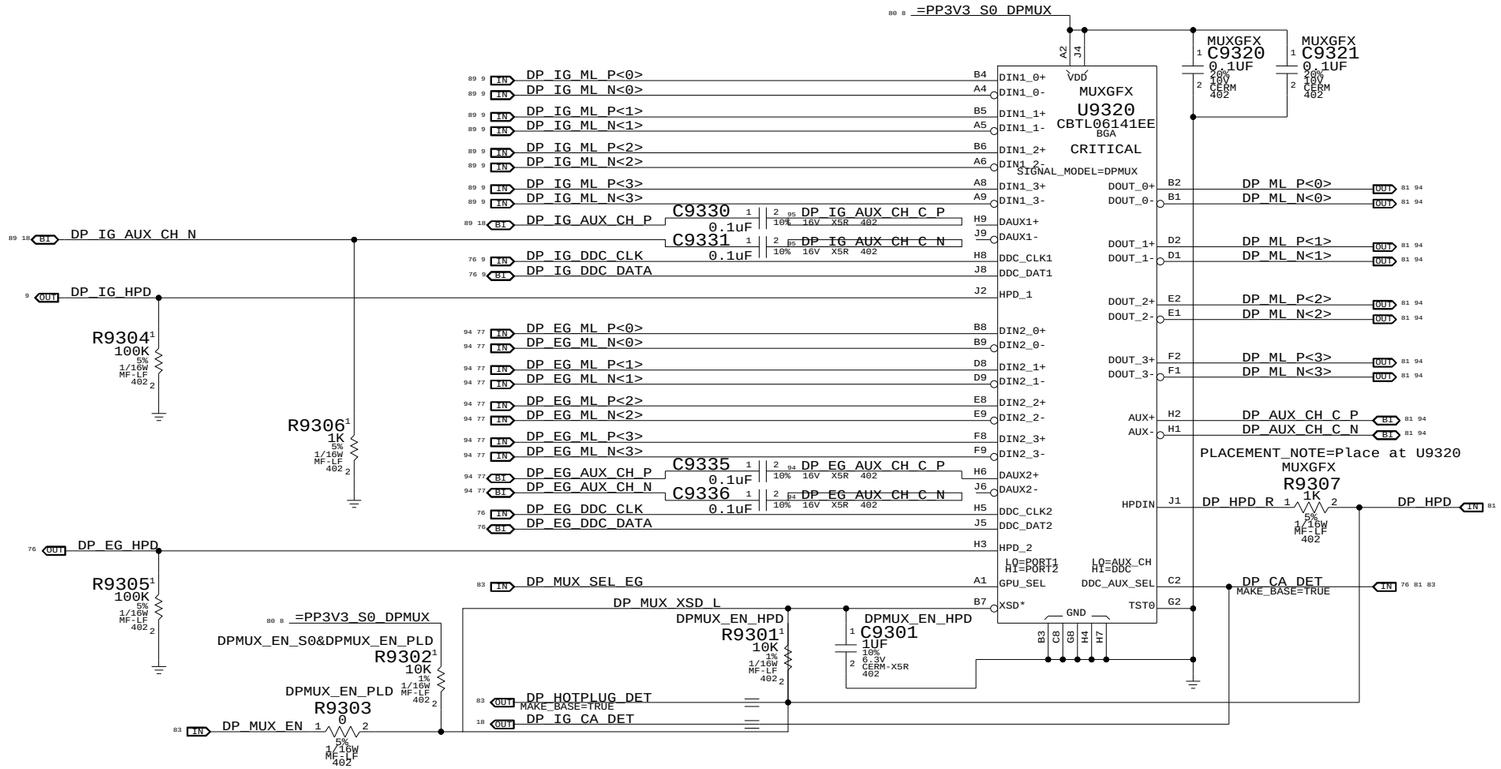
# LVDS Transmitter Termination

All emulated LVDS outputs require this termination

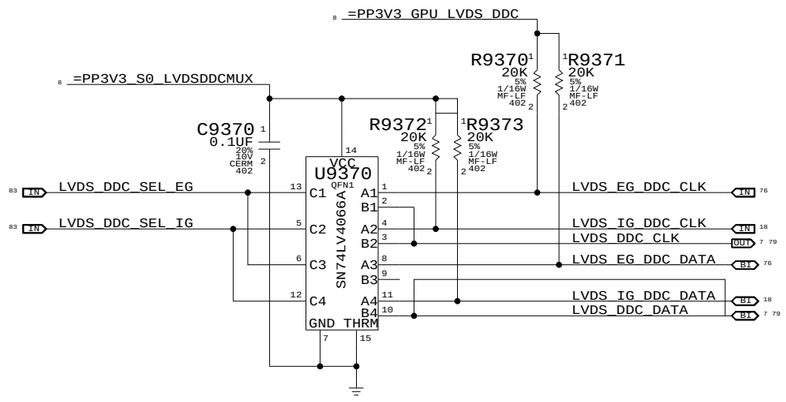
**PLACEMENT_NOTE=Place at U9200** (All 24 resistors)




# DisplayPort Mux




# LVDS DDC MUX




## Muxed Graphics Support

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008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|---|---|---|
| D | 051-7902 | D |
| SCALE: NONE | SHT 93 OF 109 | |

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# Port Power Switch

U9480 TPS2051B SOT23 (CRITICAL)
=PP3V3_S5_DP_PORT_PWR, PM_SLP_S3_L → PP3V3_S0_DPILIM, TP_DPPWR_OC_L
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
C9486 22UF 20% 6.3V X5R-CERM 603 (CRITICAL)
L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
R9420 100K 5% 1/10W MF-LF 402

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402
R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402

HDMI_CEC
R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402
FL9403 12-OHM-100MA TCM1210-4SM

DP_ML_P<3> → C9414 0.1uF 10% 16V X5R 402 → DP_ML_C_P<3>
DP_ML_N<3> → C9415 0.1uF 10% 16V X5R 402 → DP_ML_C_N<3>
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

OMIT CRITICAL J9400 DSPLYPRT-M97 F-RT-THSM

| BOT ROW TH PINS | | TOP ROW SM PINS |
|---|---|---|
| 2 | HOT_PLUG_DETECT | 1 GND |
| 4 | CONFIG1 | 3 ML_LANE0P |
| 6 | CONFIG2 | 5 ML_LANE0N |
| 8 | GND | 7 GND |
| 10 | ML_LANE3P | 9 ML_LANE1P |
| 12 | ML_LANE3N | 11 ML_LANE1N |
| 14 | GND | 13 GND |
| 16 | AUX_CHP | 15 ML_LANE2P |
| 18 | AUX_CHN | 17 ML_LANE2N |
| 20 | DP_PWR | 19 RETURN |
| | SHIELD PINS | 22 21 |

DP_ML_CONN_P<0> → FL9401 → DP_ML_C_P<0> → C9410 0.1uF → DP_ML_P<0>
DP_ML_CONN_N<0> → FL9401 → DP_ML_C_N<0> → C9411 0.1uF → DP_ML_N<0>
DP_ML_CONN_P<1> → FL9401 → DP_ML_C_P<1> → C9412 0.1uF → DP_ML_P<1>
DP_ML_CONN_N<1> → FL9401 → DP_ML_C_N<1> → C9413 0.1uF → DP_ML_N<1>
DP_ML_CONN_P<2> → FL9402 → DP_ML_C_P<2> → C9416 0.1uF → DP_ML_P<2>
DP_ML_CONN_N<2> → FL9402 → DP_ML_C_N<2> → C9417 0.1uF → DP_ML_N<2>

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1
DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET → Q9440 2N7002DW-X-G SOT-363 → DP_CA_DET_L_Q → Q9440 → DP_CA_DET_Q
R9421 100K 5% 1/16W MF-LF 402
R9422 1M 5% 1/16W MF-LF 402

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD → Q9441 2N7002DW-X-G SOT-363 → DP_HPD_L_Q → Q9441 → DP_HPD_Q
R9423 100K 5% 1/16W MF-LF 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 514-0637 | 1 | CONN,RCP,MDP,HB,20P,P=0.6 | J9400 | CRITICAL | |

## DisplayPort Connector

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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| D | 051-7902 | D |
| SCALE: NONE | SHT 94 OF 109 | |

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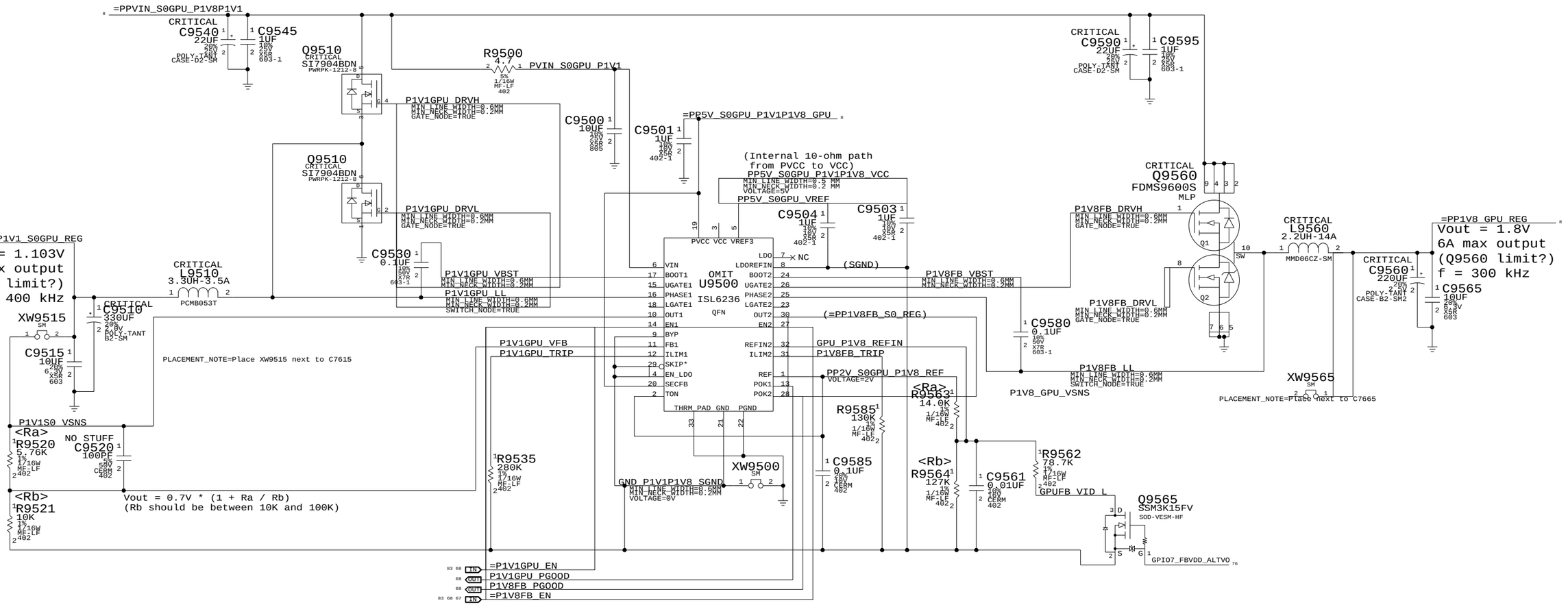


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S2312 | 1 | IC,ISL6236,DUAL PWM CTRL,QFN32 | U9500 | CRITICAL | |

# 1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008


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|---|---|---|
| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 95 | 109 |

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# GMUX CPLD

=PP3V3_S0_GMUX
=PP2V5_S0_GMUX
=PP1V2_S0_GMUX

C9610 C9621 C9622 C9623 C9624 C9625 C9626 C9628 C9629 C9630 0.1UF 20% 10V CERM 402

C9611 C9612 C9613 C9614 C9615 C9616 C9617 0.1UF 20% 10V CERM 402

C9600 4.7UF 20% 10V X5R 402

C9604 C9605 C9606 C9607 C9608 C9609 0.1UF 20% 10V CERM 402

L9631 FERR-220-OHM 0402
PP3V3_S0_ULC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9631 0.1UF 20% 10V CERM 402

L9627 FERR-220-OHM 0402
PP3V3_S0_LRC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9627 0.1UF 20% 10V CERM 402

R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402
NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402
NO STUFF R9647 10K 1% 1/16W MF-LF 402

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO6 B5 · VCCIO1 B7 · VCCIO2 A12 · VCCIO3 C14 · VCCIO4 F13 · VCCIO5 M12 · VCCIO6 M9 · VCCIO7 M3 · VCCJ N5 · ULC_VCCPLL M1 · LRC_VCCPLL C3 · A4 F2 · P11 K12

OMIT CRITICAL
U9600 XP28 CSBGA-HF

| | | | | |
|---|---|---|---|---|
| JTAG_GMUX_TCK | K14 | TCK | | |
| JTAG_GMUX_TDI | L13 | TDI | IN | |
| JTAG_GMUX_TDO | K13 | TDO | OUT | |
| JTAG_GMUX_TMS | L12 | TMS | IN | |
| GMUX_TOE | K2 | TOE | | |
| GMUX_CFG0 | K1 | CFG0 | | |
| LCD_BKLT_EN | P2 | PB2A | OUT | |
| LCD_BKLT_PWM | N2 | PB2B | OUT | |
| LVDS_DDC_SEL_EG | P4 | PB14A | OUT | |
| LVDS_DDC_SEL_IG | N4 | PB14B | OUT | |
| DP_MUX_EN | N3 | PB15A | OUT | (OD) |
| DP_MUX_SEL_EG | M4 | PB15B | OUT | |
| EG_RESET_L | P5 | PB16A | OUT | |
| EG_RAIL1_EN | M5 | PB16B | OUT | |
| EG_RAIL2_EN | P6 | PB17A | OUT | |
| EG_RAIL3_EN | M6 | PB17B | OUT | |
| EG_RAIL4_EN | P7 | PB18A | OUT | |
| EG_CLKREQ_OUT_L | M7 | PB18B | OUT | (OD) |
| DP_CA_DET_EG | N7 | PB19A | OUT | |
| LCD_PWR_EN | N8 | PB19B | OUT | |
| LPC_AD<0> | P9 | PB20A | BI | |
| LPC_AD<1> | N9 | PB20B | BI | |
| LPC_AD<2> | P10 | PB30A | BI | |
| LPC_AD<3> | M10 | PB30B | BI | |
| LPC_FRAME_L | P12 | PB31A | BI | |
| LPC_RESET_L | P13 | PB31B | IN | |
| LPC_CLK33M_GMUX | N12 | PB32A | IN | |
| GMUX_INT | P14 | PB32B | OUT | |
| LVDS_IG_B_DATA_P<2> | B1 | PL2A | IN | |
| LVDS_IG_B_DATA_N<2> | B2 | PL2B | IN | |
| TP_GMUX_PL10A | C2 | PL10A | | |
| TP_GMUX_PL10B | D3 | PL10B | | |
| LVDS_IG_A_DATA_P<0> | D1 | PL11A | IN | |
| LVDS_IG_A_DATA_N<0> | E1 | PL11B | IN | |
| LVDS_IG_A_DATA_P<1> | D2 | PL12A | IN | |
| LVDS_IG_A_DATA_N<1> | E3 | PL12B | IN | |
| LVDS_IG_A_DATA_P<2> | F1 | PL13A | IN | |
| LVDS_IG_A_DATA_N<2> | G1 | PL13B | IN | |
| LVDS_IG_B_DATA_P<0> | F3 | PL14A | IN | |
| LVDS_IG_B_DATA_N<0> | G2 | PL14B | IN | |
| LVDS_IG_B_DATA_P<1> | H2 | PL15A | IN | |
| LVDS_IG_B_DATA_N<1> | G3 | PL15B | IN | |
| LVDS_IG_A_CLK_P | H1 | PL16A | IN | |
| LVDS_IG_A_CLK_N | H3 | PL16B | IN | |
| LVDS_MUX_SEL_EG | L1 | PL18A | OUT | |
| TP_GMUX_PL18B_VSYNC | L3 | PL18B | | |
| =GMUX_PCIE_RESET_L | K3 | PL19A | IN | |
| GMUX_PM_SLP_S3_L | L2 | PL19B | IN | |
| ALL_EG_PGOOD | N1 | PL32A | IN | |
| EG_CLKREQ_IN_L | P1 | PL32B | IN | |

BANK5 · BANK4 · BANK7 · BANK6

GND: J1 B8 C6 C12 C13 E13 M14 N10 N6 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

BANK0

| | | | | |
|---|---|---|---|---|
| PT2A | A2 | LVDS_B_DATA_P<0> | OUT | 80 94 |
| PT2B | A3 | LVDS_B_DATA_N<0> | OUT | 80 94 |
| PT3A | A1 | LVDS_B_DATA_P<1> | OUT | 80 94 |
| PT3B | B3 | LVDS_B_DATA_N<1> | OUT | 80 94 |
| PT4A | C5 | LVDS_B_DATA_P<2> | OUT | 80 94 |
| PT4B | A5 | LVDS_B_DATA_N<2> | OUT | 80 94 |
| PT14A | B6 | EG_PWRSEQ_EN | IN | 83 |
| PT14B | C7 | GMUX_DEBUG_RESET_L | IN | 83 |
| PT15A | A6 | LVDS_A_CLK_P | OUT | 80 94 |
| PT15B | A7 | LVDS_A_CLK_N | OUT | 80 94 |
| PT16A | C8 | LVDS_B_CLK_P | OUT | 80 94 |
| PT16B | C9 | LVDS_B_CLK_N | OUT | 80 94 |
| PT17A | A8 | LVDS_A_DATA_P<0> | OUT | 80 94 |
| PT17B | B9 | LVDS_A_DATA_N<0> | OUT | 80 94 |
| PT18A | A9 | LVDS_A_DATA_P<1> | OUT | 80 94 |
| PT18B | C10 | LVDS_A_DATA_N<1> | OUT | 80 94 |
| PT19A | B10 | LVDS_A_DATA_P<2> | OUT | 80 94 |
| PT19B | A10 | LVDS_A_DATA_N<2> | OUT | 80 94 |

BANK1

| | | | | |
|---|---|---|---|---|
| PT20A | A11 | TP_GMUX_PT20A | | |
| PT20B | B12 | TP_GMUX_PT20B | | |
| PT32A | B13 | TP_GMUX_PT32A | | |
| PT32B | A13 | TP_GMUX_PT32B | | |

BANK2

| | | | | |
|---|---|---|---|---|
| PR2A | A14 | DP_CA_DET | IN | 76 80 81 |
| PR2B | B14 | DP_HOTPLUG_DET | IN | 80 |
| PR10A | D12 | LVDS_EG_A_DATA_P<0> | IN | 77 83 94 |
| PR10B | D13 | LVDS_EG_A_DATA_N<0> | IN | 77 83 94 |
| PR11A | D14 | LVDS_EG_A_DATA_P<1> | IN | 77 83 94 |
| PR11B | E14 | LVDS_EG_A_DATA_N<1> | IN | 77 83 94 |
| PR12A | E12 | LVDS_EG_A_DATA_P<2> | IN | 77 83 94 |
| PR12B | F12 | LVDS_EG_A_DATA_N<2> | IN | 77 83 94 |
| PR13A | F14 | LVDS_EG_B_DATA_P<0> | IN | 77 83 94 |
| PR13B | G14 | LVDS_EG_B_DATA_N<0> | IN | 77 83 94 |
| PR14A | G12 | LVDS_EG_B_DATA_P<1> | IN | 77 83 94 |
| PR14B | G13 | LVDS_EG_B_DATA_N<1> | IN | 77 83 94 |
| PR15A | H13 | LVDS_EG_B_DATA_P<2> | IN | 77 83 94 |
| PR15B | H12 | LVDS_EG_B_DATA_N<2> | IN | 77 83 94 |
| PR16A | H14 | LVDS_EG_A_CLK_P | IN | 77 83 94 |
| PR16B | J12 | LVDS_EG_A_CLK_N | IN | 77 83 94 |
| PR18A | L14 | IG_LCD_PWR_EN | IN | 9 |
| PR18B | M13 | EG_LCD_PWR_EN | IN | 76 |
| PR30A | N14 | IG_BKLT_EN | IN | 9 |
| PR30B | N13 | EG_BKLT_EN | IN | 76 |

BANK3

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

## PM_SLP_S3_L Isolation

=PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
PM_SLP_S3_L
EG_PWRSEQ_EN
GMUX_PM_SLP_S3_L
MAKE_BASE=TRUE

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 336S0027 | 1 | IC,XP2-8,HF,CPLD,BLANK | U9600 | CRITICAL | GMUX_8K_BLANK |
| 341S2350 | 1 | IC,CPLD,LATTICE,132CSBGA,M98 | U9600 | CRITICAL | GMUX_PROG |

## GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L

# LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

| | | | |
|---|---|---|---|
| LVDS_IG_A_CLK_P | R9650 | 100 | LVDS_IG_A_CLK_N |
| LVDS_IG_A_DATA_P<0> | R9651 | 100 | LVDS_IG_A_DATA_N<0> |
| LVDS_IG_A_DATA_P<1> | R9652 | 100 | LVDS_IG_A_DATA_N<1> |
| LVDS_IG_A_DATA_P<2> | R9653 | 100 | LVDS_IG_A_DATA_N<2> |
| LVDS_IG_B_DATA_P<0> | R9654 | 100 | LVDS_IG_B_DATA_N<0> |
| LVDS_IG_B_DATA_P<1> | R9655 | 100 | LVDS_IG_B_DATA_N<1> |
| LVDS_IG_B_DATA_P<2> | R9656 | 100 | LVDS_IG_B_DATA_N<2> |
| LVDS_EG_A_CLK_P | R9660 | 100 | LVDS_EG_A_CLK_N |
| LVDS_EG_A_DATA_P<0> | R9661 | 100 | LVDS_EG_A_DATA_N<0> |
| LVDS_EG_A_DATA_P<1> | R9662 | 100 | LVDS_EG_A_DATA_N<1> |
| LVDS_EG_A_DATA_P<2> | R9663 | 100 | LVDS_EG_A_DATA_N<2> |
| LVDS_EG_B_DATA_P<0> | R9664 | 100 | LVDS_EG_B_DATA_N<0> |
| LVDS_EG_B_DATA_P<1> | R9665 | 100 | LVDS_EG_B_DATA_N<1> |
| LVDS_EG_B_DATA_P<2> | R9666 | 100 | LVDS_EG_B_DATA_N<2> |

All: 1% 1/16W MF-LF 402

SIGNAL_MODEL=EMPTY

# Required Pullups

=PP3V3_S0_GMUX

| | | | |
|---|---|---|---|
| GMUX_DEBUG_RESET_L | R9680 | 1K | 5% 1/16W MF-LF 402 |
| JTAG_GMUX_TCK | R9690 | 4.7K | 5% 1/16W MF-LF 402 |
| EG_CLKREQ_OUT_L | R9695 | 10K | 5% 1/16W MF-LF 402 |

NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

# Required Pulldowns

| | | | |
|---|---|---|---|
| DP_MUX_SEL_EG | R9681 | 10K | 5% 1/16W MF-LF 402 |
| LVDS_DDC_SEL_IG | R9682 | 10K | 5% 1/16W MF-LF 402 |
| LVDS_DDC_SEL_EG | R9683 | 10K | 5% 1/16W MF-LF 402 |

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF

| | | | |
|---|---|---|---|
| EG_RESET_L | R9691 | 100K | 5% 1/16W MF-LF 402 |
| GMUX_INT | R9692 | 20K | 5% 1/16W MF-LF 402 |
| LCD_BKLT_PWM | R9693 | 100K | 5% 1/16W MF-LF 402 |
| EG_CLKREQ_IN_L | R9694 | 100K | 5% 1/16W MF-LF 402 |

| | | | |
|---|---|---|---|
| EG_RAIL1_EN | R9630 | EG_PWRSEQ_HW | EXTGPU_PWR_EN |
| EG_RAIL1_EN | R9631 | EG_PWRSEQ_GMUX | =P1V1GPU_EN |
| EG_RAIL2_EN | R9632 | EG_PWRSEQ_GMUX | P3V3GPU_EN |
| EG_RAIL3_EN | R9633 | EG_PWRSEQ_GMUX | =GPUVCORE_EN |
| EG_RAIL4_EN | R9634 | EG_PWRSEQ_GMUX | =P1V8FB_EN |

0 5% 1/16W MF-LF 402

The MAKE BASE properties for these signals are on the POWER CONTROL page.

NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

# Graphics MUX (GMUX)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008


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| SCALE: NONE | SHT 96 OF 109 | |

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*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
R9730 0
PPVIN_S0_LCDBKLT_BUF
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVOUT_S0_LCDBKLT_SW
D9701 DX022-SM STPS1H100MF
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near C9710
PLACEMENT_NOTE=Place near J9000
CRITICAL C9701 10UF
PLACEMENT_NOTE=Place near L9701
R9701 100
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near PPVOUT_S0_LCDBKLT_SW
BKL_VIN
BOOST_FET_CNTL
Q9701 FDC5612 SSOT6
CRITICAL C9709 2.2UF
CRITICAL C9710 2.2UF
XW9701 SM
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9701
C9702 0.1UF
4 PLACEMENT_NOTE=Place near C9709
BOOST_SINK
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9709 and Q9701
R9704 100
R9702 0.4
R9715 0.4
XW9702 SM
GND_BKL_PWRGND_X
PLACEMENT_NOTE=Place near C9709 and Q9701
BKL_VREF_4V9
R9731 187K
BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0
BKL_VSYNC
R9706 10K
R9707 3.01K
C9703 1UF
C9713 0.1UF
R9705 100K
*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
C9712 47PF NOSTUFF
U9701 APP001A OMIT
PPVOUT_S0_LCDBKLT
PLACEMENT_NOTE=Away from Q9701
BKL_ISET
BKL_RT
BKL_SSTCMP
BKL_DIM
BKL_LPF
BKL_LRT
BKL_ISWSEN
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSEN
R9717 0
R9718 0
R9719 0
R9720 0
R9721 0
R9722 0
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
R9708 100K
R9709 1K
NOSTUFF R9703 2.0M
BKL_SSTCMP_RC
C9705 0.1UF
BKLT_PWM_RC
R9733 0
C9706 0.0022UF NOSTUFF
C9714 1UF NOSTUFF
R9713 0
BKLT_PLL_NOT
R9714 10K
R9727 15.0K
C9707 2.2UF
BKLT_PLL_RC
C9708 0.1UF
CRITICAL Q9702 NTUD3127CXXG SOT-963
BKL_VREF_IN_4V9
R9700 100K
BKL_PWR_EN_L
R9710 10K
CRITICAL Q9702 N-CHN NTUD3127CXXG SOT-963
LCD_BKLT_PWM
R9711 30.1K
R9723 1.2M
R9724 71.5K

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S2413 | 1 | IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20 | U9701 | CRITICAL | |

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER
SYNC_MASTER=YITE_M98_MLB
SYNC_DATE=07/02/2008

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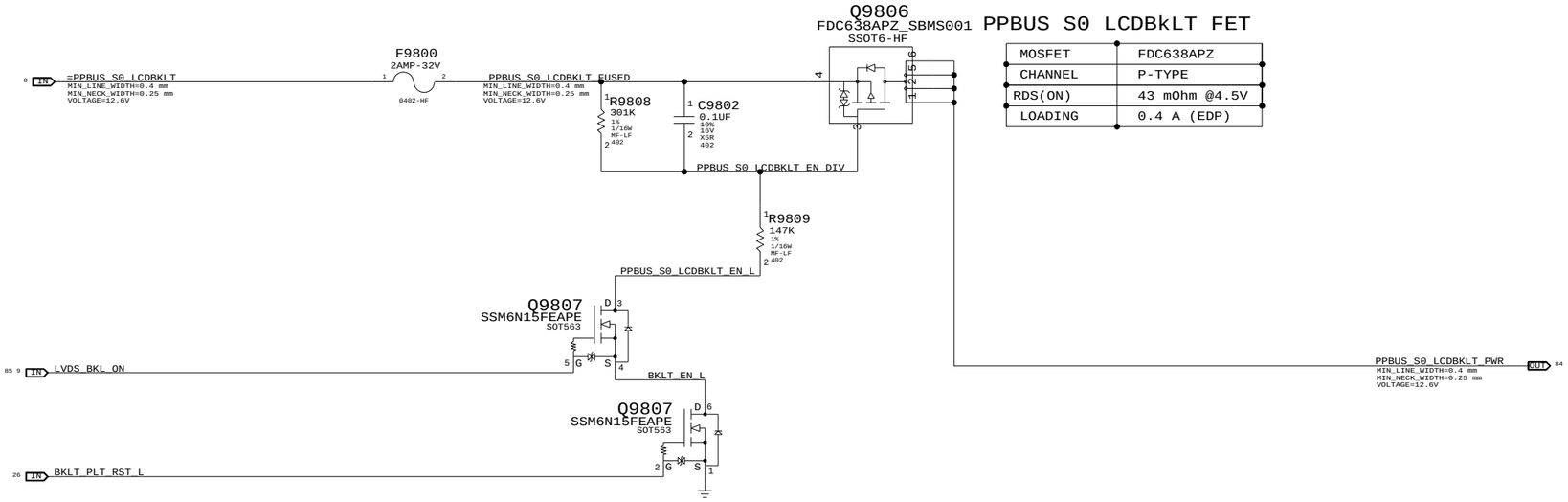


| | |
|---|---|
| MOSFET | FDC638APZ |
| CHANNEL | P-TYPE |
| RDS(ON) | 43 mOhm @4.5V |
| LOADING | 0.4 A (EDP) |

LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008


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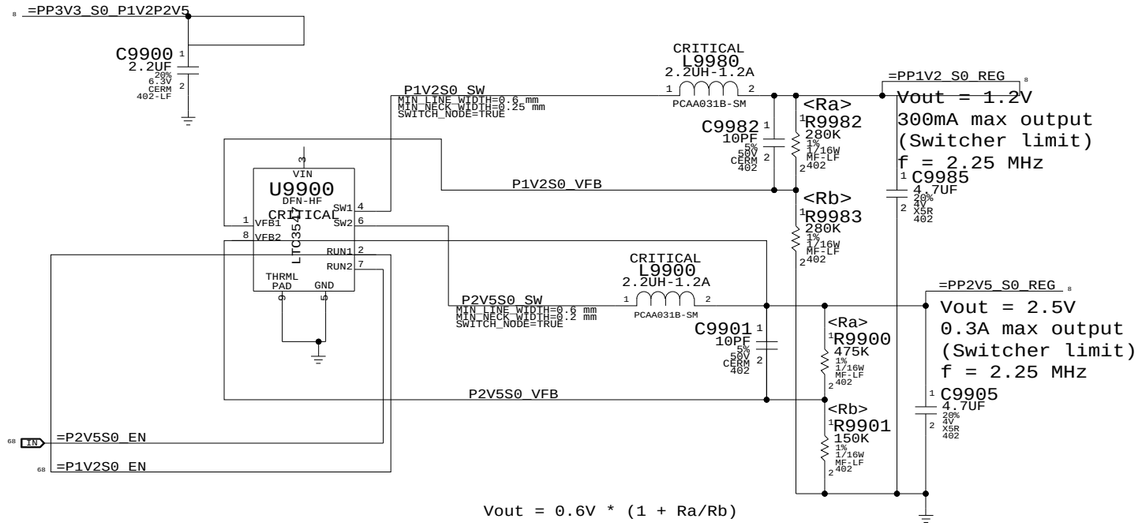
# 2.5V/1.2V S3 Switcher




## Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008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# FSB (Front-Side Bus) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| FSB_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| FSB_DSTB_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| FSB_DATA | * | =2x_DIELECTRIC | ? |
| FSB_DSTB | * | =3x_DIELECTRIC | ? |
| FSB_ADDR | * | =STANDARD | ? |
| FSB_ADSTB | * | =2x_DIELECTRIC | ? |
| FSB_1X | * | =STANDARD | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| FSB_DATA | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| FSB_DSTB | TOP,BOTTOM | =5x_DIELECTRIC | ? |
| FSB_ADDR | TOP,BOTTOM | =3x_DIELECTRIC | ? |
| FSB_ADSTB | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| FSB_1X | TOP,BOTTOM | =3x_DIELECTRIC | ? |

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

# CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CPU_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CPU_27P4S | * | =27P4_OHM_SE | =27P4_OHM_SE | =27P4_OHM_SE | =27P4_OHM_SE | 7 MIL | 7 MIL |

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CPU_AGTL | * | =STANDARD | ? |
| CPU_8MIL | * | 8 MIL | ? |
| CPU_COMP | * | 25 MIL | ? |
| CPU_GTLREF | * | 25 MIL | ? |
| CPU_ITP | * | =2:1_SPACING | ? |
| CPU_VCCSENSE | * | 25 MIL | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CPU_AGTL | TOP,BOTTOM | =2x_DIELECTRIC | ? |

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

# MCP FSB COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MCP_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MCP_FSB_COMP | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

# FSB Clock Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_FSB_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_FSB | * | =3x_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_FSB | TOP,BOTTOM | =4x_DIELECTRIC | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

# CPU / FSB Net Properties

| | ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|---|
| FSB 4X Signal Groups | FSB_DATA_GROUP0 | FSB_50S | FSB_DATA | FSB_D_L<15..0> | 7 10 14 |
| | FSB_DATA_GROUP0 | FSB_50S | FSB_DATA | FSB_DINV_L<0> | 7 10 14 |
| | FSB_DSTB0 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_P<0> | 7 10 14 |
| | FSB_DSTB0 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_N<0> | 7 10 14 |
| | FSB_DATA_GROUP1 | FSB_50S | FSB_DATA | FSB_D_L<31..16> | 7 10 14 |
| | FSB_DATA_GROUP1 | FSB_50S | FSB_DATA | FSB_DINV_L<1> | 7 10 14 |
| | FSB_DSTB1 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_P<1> | 7 10 14 |
| | FSB_DSTB1 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_N<1> | 7 10 14 |
| | FSB_DATA_GROUP2 | FSB_50S | FSB_DATA | FSB_D_L<47..32> | 7 10 14 |
| | FSB_DATA_GROUP2 | FSB_50S | FSB_DATA | FSB_DINV_L<2> | 7 10 14 |
| | FSB_DSTB2 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_P<2> | 7 10 14 |
| | FSB_DSTB2 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_N<2> | 7 10 14 |
| | FSB_DATA_GROUP3 | FSB_50S | FSB_DATA | FSB_D_L<63..48> | 7 10 14 |
| | FSB_DATA_GROUP3 | FSB_50S | FSB_DATA | FSB_DINV_L<3> | 7 10 14 |
| | FSB_DSTB3 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_P<3> | 7 10 14 |
| | FSB_DSTB3 | FSB_DSTB_50S | FSB_DSTB | FSB_DSTB_L_N<3> | 7 10 14 |
| FSB 2X Signals | FSB_ADDR_GROUP0 | FSB_50S | FSB_ADDR | FSB_A_L<16..3> | 7 10 14 |
| | FSB_ADDR_GROUP0 | FSB_50S | FSB_ADDR | FSB_REQ_L<4..0> | 7 10 14 |
| | FSB_ADSTB0 | FSB_50S | FSB_ADSTB | FSB_ADSTB_L<0> | 7 10 14 |
| | FSB_ADDR_GROUP1 | FSB_50S | FSB_ADDR | FSB_A_L<35..17> | 7 10 14 |
| | FSB_ADSTB1 | FSB_50S | FSB_ADSTB | FSB_ADSTB_L<1> | 7 10 14 |
| FSB 1X Signals | FSB_1X | FSB_50S | FSB_1X | FSB_ADS_L | 7 10 14 |
| | FSB_BREQ0_L | FSB_50S | FSB_1X | FSB_BREQ0_L | 9 10 14 |
| | FSB_BREQ1_L | FSB_50S | FSB_1X | FSB_BREQ1_L | 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_BNR_L | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_BPRI_L | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_DBSY_L | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_DEFER_L | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_DRDY_L | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_HIT_L | 7 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_HITM_L | 7 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_LOCK_L | 7 10 14 |
| | FSB_CPURST_L | FSB_50S | FSB_1X | FSB_CPURST_L | 9 10 13 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_RS_L<2..0> | 10 14 |
| | FSB_1X | FSB_50S | FSB_1X | FSB_TRDY_L | 10 14 |
| | CPU_ASYNC | CPU_50S | CPU_AGTL | CPU_A20M_L | 10 14 |
| | CPU_BSEL | CPU_50S | CPU_AGTL | CPU_BSEL<2..0> | 9 10 |
| | CPU_FERR_L | CPU_50S | CPU_8MIL | CPU_FERR_L | 10 14 |
| | CPU_ASYNC | CPU_50S | CPU_AGTL | CPU_IGNNE_L | 10 14 |
| | CPU_INIT_L | CPU_50S | CPU_AGTL | CPU_INIT_L | 10 14 |
| | CPU_ASYNC_R | CPU_50S | CPU_AGTL | CPU_INTR | 9 10 14 |
| | CPU_ASYNC_R | CPU_50S | CPU_AGTL | CPU_NMI | 9 10 14 |
| | CPU_PROCHOT_L | CPU_50S | CPU_AGTL | CPU_PROCHOT_L | 10 14 43 62 |
| | CPU_PWRGD | CPU_50S | CPU_AGTL | CPU_PWRGD | 10 13 14 |
| | CPU_ASYNC | CPU_50S | CPU_AGTL | CPU_SMI_L | 10 14 |
| | CPU_ASYNC | CPU_50S | CPU_AGTL | CPU_STPCLK_L | 10 14 |
| | PM_THRMTRIP_L | CPU_50S | CPU_8MIL | PM_THRMTRIP_L | 10 14 43 |
| | FSB_CPUSLP_L | CPU_50S | CPU_AGTL | FSB_CPUSLP_L | 10 14 |
| | CPU_FROM_SB | CPU_50S | CPU_AGTL | CPU_DPSLP_L | 10 14 |
| | CPU_DPRSTP_L | CPU_50S | CPU_AGTL | CPU_DPRSTP_L | 9 10 14 62 |
| | CPU_ASYNC | CPU_50S | CPU_AGTL | FSB_DPWR_L | 10 14 |
| | MCP_CPU_COMP | MCP_50S | MCP_FSB_COMP | MCP_BCLK_VML_COMP_VDD | 14 |
| | MCP_CPU_COMP | MCP_50S | MCP_FSB_COMP | MCP_BCLK_VML_COMP_GND | 14 |
| | MCP_CPU_COMP | MCP_50S | MCP_FSB_COMP | MCP_CPU_COMP_VCC | 14 |
| | MCP_CPU_COMP | MCP_50S | MCP_FSB_COMP | MCP_CPU_COMP_GND | 14 |
| | FSB_CLK_CPU | CLK_FSB_100D | CLK_FSB | FSB_CLK_CPU_P | 10 14 |
| | FSB_CLK_CPU | CLK_FSB_100D | CLK_FSB | FSB_CLK_CPU_N | 10 14 |
| | FSB_CLK_ITP | CLK_FSB_100D | CLK_FSB | FSB_CLK_ITP_P | 13 14 |
| | FSB_CLK_ITP | CLK_FSB_100D | CLK_FSB | FSB_CLK_ITP_N | 13 14 |
| | FSB_CLK_MCP | CLK_FSB_100D | CLK_FSB | FSB_CLK_MCP_P | 14 |
| | FSB_CLK_MCP | CLK_FSB_100D | CLK_FSB | FSB_CLK_MCP_N | 14 |
| | CPU_IERR_L | CPU_50S | | CPU_IERR_L | 10 |
| | PM_DPRSLPVR | CPU_50S | CPU_AGTL | PM_DPRSLPVR | 21 62 |
| | (See above) | CPU_50S | CPU_AGTL | IMVP_DPRSLPVR | 62 |
| | CPU_GTLREF | CPU_50S | CPU_GTLREF | CPU_GTLREF | 10 27 |
| | CPU_COMP | CPU_50S | CPU_COMP | CPU_COMP<3> | 10 |
| | CPU_COMP | CPU_27P4S | CPU_COMP | CPU_COMP<2> | 10 |
| | CPU_COMP | CPU_50S | CPU_COMP | CPU_COMP<1> | 10 |
| | CPU_COMP | CPU_27P4S | CPU_COMP | CPU_COMP<0> | 10 |
| | XDP_TDI | CPU_50S | CPU_ITP | XDP_TDI | 6 10 13 |
| | XDP_TDO | CPU_50S | CPU_ITP | XDP_TDO | 6 10 |
| | XDP_TMS | CPU_50S | CPU_ITP | XDP_TMS | 6 10 13 |
| | XDP_TCK | CPU_50S | CPU_ITP | XDP_TCK | 6 10 13 |
| | XDP_TRST_L | CPU_50S | CPU_ITP | XDP_TRST_L | 6 10 13 |
| | XDP_BPM_L | CPU_50S | CPU_ITP | XDP_BPM_L<4..0> | 10 13 |
| | XDP_BPM_L5 | CPU_50S | CPU_ITP | XDP_BPM_L<5> | 10 13 |
| | (FSB_CPURST_L) | CPU_50S | CPU_ITP | XDP_CPURST_L | 13 |
| | | CPU_50S | CPU_8MIL | CPU_VID<6..0> | 9 11 |
| | | CPU_50S | CPU_8MIL | IMVP6_VID<6..0> | 9 62 |
| | CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | CPU_VCCSENSE_P | 11 62 |
| | CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | CPU_VCCSENSE_N | 11 62 |
| | (CPU_VCCSENSE) | CPU_27P4S | CPU_VCCSENSE | IMVP6_VSEN_P | 62 |
| | (CPU_VCCSENSE) | CPU_27P4S | CPU_VCCSENSE | IMVP6_VSEN_N | 62 |

# CPU/FSB Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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# Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_40S | * | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =STANDARD | =STANDARD |
| MEM_40S_VDD | * | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =STANDARD | =STANDARD |
| MEM_70D | * | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF |
| MEM_70D_VDD | * | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MEM_CLK2MEM | * | =4:1_SPACING | ? |
| MEM_CTRL2CTRL | * | =2:1_SPACING | ? |
| MEM_CTRL2MEM | * | =2.5:1_SPACING | ? |
| MEM_CMD2CMD | * | =1.5:1_SPACING | ? |
| MEM_CMD2MEM | * | =3:1_SPACING | ? |
| MEM_DATA2DATA | * | =1.5:1_SPACING | ? |
| MEM_DATA2MEM | * | =3:1_SPACING | ? |
| MEM_DQS2MEM | * | =3:1_SPACING | ? |
| MEM_2OTHER | * | 25 MIL | ? |

# Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CLK | MEM_CLK | * | MEM_CLK2MEM |
| MEM_CLK | MEM_CTRL | * | MEM_CLK2MEM |
| MEM_CLK | MEM_CMD | * | MEM_CLK2MEM |
| MEM_CLK | MEM_DATA | * | MEM_CLK2MEM |
| MEM_CLK | MEM_DQS | * | MEM_CLK2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CMD | MEM_CLK | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CTRL | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CMD | * | MEM_CMD2CMD |
| MEM_CMD | MEM_DATA | * | MEM_CMD2MEM |
| MEM_CMD | MEM_DQS | * | MEM_CMD2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CTRL | MEM_CLK | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_CTRL | * | MEM_CTRL2CTRL |
| MEM_CTRL | MEM_CMD | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_DATA | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_DQS | * | MEM_CTRL2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DATA | MEM_CLK | * | MEM_DATA2MEM |
| MEM_DATA | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DATA | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DATA | MEM_DATA | * | MEM_DATA2DATA |
| MEM_DATA | MEM_DQS | * | MEM_DATA2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQS | MEM_CLK | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CTRL | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CMD | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DATA | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQS | * | MEM_DQS2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CLK | * | * | MEM_2OTHER |
| MEM_CTRL | * | * | MEM_2OTHER |
| MEM_CMD | * | * | MEM_2OTHER |
| MEM_DATA | * | * | MEM_2OTHER |
| MEM_DQS | * | * | MEM_2OTHER |

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

# MCP MEM COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MCP_MEM_COMP | * | Y | 7 MIL | 7 MIL | =STANDARD | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MCP_MEM_COMP | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

# Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| MEM_A_CLK | MEM_70D_VDD | MEM_CLK | MEM_A_CLK_P<5..0> | 15 28 |
| MEM_A_CLK | MEM_70D_VDD | MEM_CLK | MEM_A_CLK_N<5..0> | 15 28 |
| MEM_A_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_A_CKE<3..0> | 15 28 |
| MEM_A_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_A_CS_L<3..0> | 15 28 |
| MEM_A_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_A_ODT<3..0> | 15 28 |
| MEM_A_CMD | MEM_40S_VDD | MEM_CMD | MEM_A_A<14..0> | 15 28 |
| MEM_A_CMD | MEM_40S_VDD | MEM_CMD | MEM_A_BA<2..0> | 15 28 |
| MEM_A_CMD | MEM_40S_VDD | MEM_CMD | MEM_A_RAS_L | 15 28 |
| MEM_A_CMD | MEM_40S_VDD | MEM_CMD | MEM_A_CAS_L | 15 28 |
| MEM_A_CMD | MEM_40S_VDD | MEM_CMD | MEM_A_WE_L | 15 28 |
| MEM_A_DQ_BYTE0 | MEM_40S | MEM_DATA | MEM_A_DQ<7..0> | 15 28 |
| MEM_A_DQ_BYTE1 | MEM_40S | MEM_DATA | MEM_A_DQ<15..8> | 15 28 |
| MEM_A_DQ_BYTE2 | MEM_40S | MEM_DATA | MEM_A_DQ<23..16> | 15 28 |
| MEM_A_DQ_BYTE3 | MEM_40S | MEM_DATA | MEM_A_DQ<31..24> | 15 28 |
| MEM_A_DQ_BYTE4 | MEM_40S | MEM_DATA | MEM_A_DQ<39..32> | 15 28 |
| MEM_A_DQ_BYTE5 | MEM_40S | MEM_DATA | MEM_A_DQ<47..40> | 15 28 |
| MEM_A_DQ_BYTE6 | MEM_40S | MEM_DATA | MEM_A_DQ<55..48> | 15 28 |
| MEM_A_DQ_BYTE7 | MEM_40S | MEM_DATA | MEM_A_DQ<63..56> | 15 28 |
| MEM_A_DQ_BYTE0 | MEM_40S | MEM_DATA | MEM_A_DM<0> | 15 28 |
| MEM_A_DQ_BYTE1 | MEM_40S | MEM_DATA | MEM_A_DM<1> | 15 28 |
| MEM_A_DQ_BYTE2 | MEM_40S | MEM_DATA | MEM_A_DM<2> | 15 28 |
| MEM_A_DQ_BYTE3 | MEM_40S | MEM_DATA | MEM_A_DM<3> | 15 28 |
| MEM_A_DQ_BYTE4 | MEM_40S | MEM_DATA | MEM_A_DM<4> | 15 28 |
| MEM_A_DQ_BYTE5 | MEM_40S | MEM_DATA | MEM_A_DM<5> | 15 28 |
| MEM_A_DQ_BYTE6 | MEM_40S | MEM_DATA | MEM_A_DM<6> | 15 28 |
| MEM_A_DQ_BYTE7 | MEM_40S | MEM_DATA | MEM_A_DM<7> | 15 28 |
| MEM_A_DQS0 | MEM_70D | MEM_DQS | MEM_A_DQS_P<0> | 15 28 |
| MEM_A_DQS0 | MEM_70D | MEM_DQS | MEM_A_DQS_N<0> | 15 28 |
| MEM_A_DQS1 | MEM_70D | MEM_DQS | MEM_A_DQS_P<1> | 15 28 |
| MEM_A_DQS1 | MEM_70D | MEM_DQS | MEM_A_DQS_N<1> | 15 28 |
| MEM_A_DQS2 | MEM_70D | MEM_DQS | MEM_A_DQS_P<2> | 15 28 |
| MEM_A_DQS2 | MEM_70D | MEM_DQS | MEM_A_DQS_N<2> | 15 28 |
| MEM_A_DQS3 | MEM_70D | MEM_DQS | MEM_A_DQS_P<3> | 15 28 |
| MEM_A_DQS3 | MEM_70D | MEM_DQS | MEM_A_DQS_N<3> | 15 28 |
| MEM_A_DQS4 | MEM_70D | MEM_DQS | MEM_A_DQS_P<4> | 15 28 |
| MEM_A_DQS4 | MEM_70D | MEM_DQS | MEM_A_DQS_N<4> | 15 28 |
| MEM_A_DQS5 | MEM_70D | MEM_DQS | MEM_A_DQS_P<5> | 15 28 |
| MEM_A_DQS5 | MEM_70D | MEM_DQS | MEM_A_DQS_N<5> | 15 28 |
| MEM_A_DQS6 | MEM_70D | MEM_DQS | MEM_A_DQS_P<6> | 15 28 |
| MEM_A_DQS6 | MEM_70D | MEM_DQS | MEM_A_DQS_N<6> | 15 28 |
| MEM_A_DQS7 | MEM_70D | MEM_DQS | MEM_A_DQS_P<7> | 15 28 |
| MEM_A_DQS7 | MEM_70D | MEM_DQS | MEM_A_DQS_N<7> | 15 28 |
| MEM_B_CLK | MEM_70D_VDD | MEM_CLK | MEM_B_CLK_P<5..0> | 15 29 |
| MEM_B_CLK | MEM_70D_VDD | MEM_CLK | MEM_B_CLK_N<5..0> | 15 29 |
| MEM_B_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_B_CKE<3..0> | 15 29 |
| MEM_B_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_B_CS_L<3..0> | 15 29 |
| MEM_B_CNTL | MEM_40S_VDD | MEM_CTRL | MEM_B_ODT<3..0> | 15 29 |
| MEM_B_CMD | MEM_40S_VDD | MEM_CMD | MEM_B_A<14..0> | 15 29 |
| MEM_B_CMD | MEM_40S_VDD | MEM_CMD | MEM_B_BA<2..0> | 15 29 |
| MEM_B_CMD | MEM_40S_VDD | MEM_CMD | MEM_B_RAS_L | 15 29 |
| MEM_B_CMD | MEM_40S_VDD | MEM_CMD | MEM_B_CAS_L | 15 29 |
| MEM_B_CMD | MEM_40S_VDD | MEM_CMD | MEM_B_WE_L | 15 29 |
| MEM_B_DQ_BYTE0 | MEM_40S | MEM_DATA | MEM_B_DQ<7..0> | 15 29 |
| MEM_B_DQ_BYTE1 | MEM_40S | MEM_DATA | MEM_B_DQ<15..8> | 15 29 |
| MEM_B_DQ_BYTE2 | MEM_40S | MEM_DATA | MEM_B_DQ<23..16> | 15 29 |
| MEM_B_DQ_BYTE3 | MEM_40S | MEM_DATA | MEM_B_DQ<31..24> | 15 29 |
| MEM_B_DQ_BYTE4 | MEM_40S | MEM_DATA | MEM_B_DQ<39..32> | 15 29 |
| MEM_B_DQ_BYTE5 | MEM_40S | MEM_DATA | MEM_B_DQ<47..40> | 15 29 |
| MEM_B_DQ_BYTE6 | MEM_40S | MEM_DATA | MEM_B_DQ<55..48> | 15 29 |
| MEM_B_DQ_BYTE7 | MEM_40S | MEM_DATA | MEM_B_DQ<63..56> | 15 29 |
| MEM_B_DQ_BYTE0 | MEM_40S | MEM_DATA | MEM_B_DM<0> | 15 29 |
| MEM_B_DQ_BYTE1 | MEM_40S | MEM_DATA | MEM_B_DM<1> | 15 29 |
| MEM_B_DQ_BYTE2 | MEM_40S | MEM_DATA | MEM_B_DM<2> | 15 29 |
| MEM_B_DQ_BYTE3 | MEM_40S | MEM_DATA | MEM_B_DM<3> | 15 29 |
| MEM_B_DQ_BYTE4 | MEM_40S | MEM_DATA | MEM_B_DM<4> | 15 29 |
| MEM_B_DQ_BYTE5 | MEM_40S | MEM_DATA | MEM_B_DM<5> | 15 29 |
| MEM_B_DQ_BYTE6 | MEM_40S | MEM_DATA | MEM_B_DM<6> | 15 29 |
| MEM_B_DQ_BYTE7 | MEM_40S | MEM_DATA | MEM_B_DM<7> | 15 29 |
| MEM_B_DQS0 | MEM_70D | MEM_DQS | MEM_B_DQS_P<0> | 15 29 |
| MEM_B_DQS0 | MEM_70D | MEM_DQS | MEM_B_DQS_N<0> | 15 29 |
| MEM_B_DQS1 | MEM_70D | MEM_DQS | MEM_B_DQS_P<1> | 15 29 |
| MEM_B_DQS1 | MEM_70D | MEM_DQS | MEM_B_DQS_N<1> | 15 29 |
| MEM_B_DQS2 | MEM_70D | MEM_DQS | MEM_B_DQS_P<2> | 15 29 |
| MEM_B_DQS2 | MEM_70D | MEM_DQS | MEM_B_DQS_N<2> | 15 29 |
| MEM_B_DQS3 | MEM_70D | MEM_DQS | MEM_B_DQS_P<3> | 15 29 |
| MEM_B_DQS3 | MEM_70D | MEM_DQS | MEM_B_DQS_N<3> | 15 29 |
| MEM_B_DQS4 | MEM_70D | MEM_DQS | MEM_B_DQS_P<4> | 15 29 |
| MEM_B_DQS4 | MEM_70D | MEM_DQS | MEM_B_DQS_N<4> | 15 29 |
| MEM_B_DQS5 | MEM_70D | MEM_DQS | MEM_B_DQS_P<5> | 15 29 |
| MEM_B_DQS5 | MEM_70D | MEM_DQS | MEM_B_DQS_N<5> | 15 29 |
| MEM_B_DQS6 | MEM_70D | MEM_DQS | MEM_B_DQS_P<6> | 15 29 |
| MEM_B_DQS6 | MEM_70D | MEM_DQS | MEM_B_DQS_N<6> | 15 29 |
| MEM_B_DQS7 | MEM_70D | MEM_DQS | MEM_B_DQS_P<7> | 15 29 |
| MEM_B_DQS7 | MEM_70D | MEM_DQS | MEM_B_DQS_N<7> | 15 29 |
| MCP_MEM_COMP | MCP_MEM_COMP | MCP_MEM_COMP | MCP_MEM_COMP_VDD | 16 |
| MCP_MEM_COMP | MCP_MEM_COMP | MCP_MEM_COMP | MCP_MEM_COMP_GND | 16 |

# Memory Constraints

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# PCI-Express

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCIE_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | 13.1 MM | =90_OHM_DIFF | =90_OHM_DIFF |
| CLK_PCIE_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE | * | =3X_DIELECTRIC | ? |
| CLK_PCIE | * | 20 MIL | ? |
| MCP_PEX_COMP | * | 8 MIL | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE | TOP,BOTTOM | =4X_DIELECTRIC | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

# Analog Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CRT_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CRT | * | =4:1_SPACING | ? |
| CRT_2CRT | * | =STANDARD | ? |
| CRT_2CLK | * | 50 MIL | ? |
| CRT_2SWITCHER | * | 250 MIL | ? |
| CRT_SYNC | * | 16 MIL | ? |
| MCP_DAC_COMP | * | =2:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CRT | CRT | * | CRT_2CRT |

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

# Digital Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DP_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| LVDS_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| MCP_DV_COMP | * | Y | 20 MIL | 20 MIL | =STANDARD | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | * | =3x_DIELECTRIC | ? |
| LVDS | * | =3x_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| LVDS | TOP,BOTTOM | =4x_DIELECTRIC | ? |

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

# SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SATA_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA | * | =4x_DIELECTRIC | ? |
| SATA_TERMP | * | 8 MIL | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA | TOP,BOTTOM | =3x_DIELECTRIC | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

| NET_TYPE | | | |
|---|---|---|---|
| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
| | PCIE_90D | PCIE | PEG_R2D_P<15..0> 70 |
| | PCIE_90D | PCIE | PEG_R2D_N<15..0> 70 |
| PEG_R2D | PCIE_90D | PCIE | PEG_R2D_C_P<15..0> 9 70 |
| | PCIE_90D | PCIE | PEG_R2D_C_N<15..0> 9 70 |
| PEG_D2R | PCIE_90D | PCIE | PEG_D2R_P<15..0> 9 70 |
| | PCIE_90D | PCIE | PEG_D2R_N<15..0> 9 70 |
| | PCIE_90D | PCIE | PEG_D2R_C_P<15..0> 70 |
| | PCIE_90D | PCIE | PEG_D2R_C_N<15..0> 70 |
| | PCIE_90D | PCIE | PCIE_MINI_R2D_P 31 95 |
| | PCIE_90D | PCIE | PCIE_MINI_R2D_N 31 95 |
| PCIE_MINI_R2D | PCIE_90D | PCIE | PCIE_MINI_R2D_C_P 17 31 |
| | PCIE_90D | PCIE | PCIE_MINI_R2D_C_N 17 31 |
| PCIE_MINI_D2R | PCIE_90D | PCIE | PCIE_MINI_D2R_P 17 31 |
| | PCIE_90D | PCIE | PCIE_MINI_D2R_N 17 31 |
| | PCIE_90D | PCIE | PCIE_FW_R2D_P 36 |
| | PCIE_90D | PCIE | PCIE_FW_R2D_N 36 |
| PCIE_FW_R2D | PCIE_90D | PCIE | PCIE_FW_R2D_C_P 17 36 |
| | PCIE_90D | PCIE | PCIE_FW_R2D_C_N 17 36 |
| PCIE_FW_D2R | PCIE_90D | PCIE | PCIE_FW_D2R_P 17 36 |
| | PCIE_90D | PCIE | PCIE_FW_D2R_N 17 36 |
| | PCIE_90D | PCIE | PCIE_FW_D2R_C_P 36 |
| | PCIE_90D | PCIE | PCIE_FW_D2R_C_N 36 |
| | PCIE_90D | PCIE | PCIE_EXCARD_R2D_P 7 32 95 |
| | PCIE_90D | PCIE | PCIE_EXCARD_R2D_N 7 32 95 |
| PCIE_EXCARD_R2D | PCIE_90D | PCIE | PCIE_EXCARD_R2D_C_P 17 32 |
| | PCIE_90D | PCIE | PCIE_EXCARD_R2D_C_N 17 32 |
| PCIE_EXCARD_D2R | PCIE_90D | PCIE | PCIE_EXCARD_D2R_P 7 17 32 |
| | PCIE_90D | PCIE | PCIE_EXCARD_D2R_N 7 17 32 |
| MCP_PE0_REFCLK | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_P 17 70 |
| | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_N 17 70 |
| MCP_PE1_REFCLK | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_P 17 31 |
| | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_N 17 31 |
| MCP_PE2_REFCLK | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_FW_P 17 36 |
| | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_FW_N 17 36 |
| MCP_PE3_REFCLK | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_P 17 32 |
| | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_N 17 32 |
| MCP_PEX_CLK_COMP | | MCP_PEX_COMP | MCP_PEX_CLK_COMP 17 |
| CRT_RED | CRT_50S | CRT | CRT_IG_R_C_PR 18 25 |
| CRT_GREEN | CRT_50S | CRT | CRT_IG_G_Y_Y 18 25 |
| CRT_BLUE | CRT_50S | CRT | CRT_IG_B_COMP_PB 18 25 |
| CRT_SYNC | CRT_50S | CRT_SYNC | CRT_IG_HSYNC 18 25 |
| CRT_SYNC | CRT_50S | CRT_SYNC | CRT_IG_VSYNC 18 25 |
| MCP_DAC_RSET | | MCP_DAC_COMP | MCP_TV_DAC_RSET 18 25 |
| MCP_DAC_VREF | | MCP_DAC_COMP | MCP_TV_DAC_VREF 18 25 |
| TMDS_IG_TXC | DP_100D | DISPLAYPORT | TMDS_IG_TXC_P |
| TMDS_IG_TXC | DP_100D | DISPLAYPORT | TMDS_IG_TXC_N |
| TMDS_IG_TXD | DP_100D | DISPLAYPORT | TMDS_IG_TXD_P<2..0> |
| TMDS_IG_TXD | DP_100D | DISPLAYPORT | TMDS_IG_TXD_N<2..0> |
| DP_ML | DP_100D | DISPLAYPORT | DP_IG_ML_P<3..0> 9 80 |
| DP_ML | DP_100D | DISPLAYPORT | DP_IG_ML_N<3..0> 9 80 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_IG_AUX_CH_P 18 80 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_IG_AUX_CH_N 18 80 |
| MCP_HDMI_RSET | MCP_DV_COMP | | MCP_HDMI_RSET 18 25 |
| MCP_HDMI_VPROBE | MCP_DV_COMP | | MCP_HDMI_VPROBE 18 25 |
| LVDS_IG_A_CLK | LVDS_100D | LVDS | LVDS_IG_A_CLK_P 18 83 |
| LVDS_IG_A_CLK | LVDS_100D | LVDS | LVDS_IG_A_CLK_N 18 83 |
| LVDS_IG_A_DATA | LVDS_100D | LVDS | LVDS_IG_A_DATA_P<2..0> 18 83 |
| LVDS_IG_A_DATA | LVDS_100D | LVDS | LVDS_IG_A_DATA_N<2..0> 18 83 |
| LVDS_IG_A_DATA3 | LVDS_100D | LVDS | LVDS_IG_A_DATA_P<3> 9 18 |
| LVDS_IG_A_DATA3 | LVDS_100D | LVDS | LVDS_IG_A_DATA_N<3> 9 18 |
| LVDS_IG_B_CLK | LVDS_100D | LVDS | LVDS_IG_B_CLK_P 9 18 |
| LVDS_IG_B_CLK | LVDS_100D | LVDS | LVDS_IG_B_CLK_N 9 18 |
| LVDS_IG_B_DATA | LVDS_100D | LVDS | LVDS_IG_B_DATA_P<2..0> 18 83 |
| LVDS_IG_B_DATA | LVDS_100D | LVDS | LVDS_IG_B_DATA_N<2..0> 18 83 |
| LVDS_IG_B_DATA3 | LVDS_100D | LVDS | LVDS_IG_B_DATA_P<3> 9 18 |
| LVDS_IG_B_DATA3 | LVDS_100D | LVDS | LVDS_IG_B_DATA_N<3> 9 18 |
| MCP_IFPAB_RSET | MCP_DV_COMP | | MCP_IFPAB_RSET 18 25 |
| MCP_IFPAB_VPROBE | | | MCP_IFPAB_VPROBE 18 25 |
| SATA_HDD_R2D | SATA_100D | SATA | SATA_HDD_R2D_C_P 20 39 |
| | SATA_100D | SATA | SATA_HDD_R2D_C_N 20 39 |
| | SATA_100D | SATA | SATA_HDD_R2D_P 39 |
| | SATA_100D | SATA | SATA_HDD_R2D_N 39 |
| SATA_HDD_D2R | SATA_100D | SATA | SATA_HDD_D2R_P 20 39 |
| | SATA_100D | SATA | SATA_HDD_D2R_N 20 39 |
| | SATA_100D | SATA | SATA_HDD_D2R_C_P 39 |
| | SATA_100D | SATA | SATA_HDD_D2R_C_N 39 |
| SATA_ODD_R2D | SATA_100D | SATA | SATA_ODD_R2D_C_P 20 39 |
| | SATA_100D | SATA | SATA_ODD_R2D_C_N 20 39 |
| | SATA_100D | SATA | SATA_ODD_R2D_P 7 39 |
| | SATA_100D | SATA | SATA_ODD_R2D_N 7 39 |
| SATA_ODD_D2R | SATA_100D | SATA | SATA_ODD_D2R_P 20 39 |
| | SATA_100D | SATA | SATA_ODD_D2R_N 20 39 |
| | SATA_100D | SATA | SATA_ODD_D2R_C_P 7 39 |
| | SATA_100D | SATA | SATA_ODD_D2R_C_N 7 39 |
| MCP_SATA_TERMP | | SATA_TERMP | MCP_SATA_TERMP 20 |

# MCP Constraints 1

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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| SCALE: NONE | SHT 102 OF 109 | |

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## PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCI | * | =STANDARD | ? |
| CLK_PCI | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

## LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| LPC | * | 6 MIL | ? |
| CLK_LPC | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

## USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MCP_USB_RBIAS | * | =STANDARD | 8 MIL | 8 MIL | =STANDARD | =STANDARD | =STANDARD |
| USB_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB | * | =2x_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB | TOP,BOTTOM | =4x_DIELECTRIC | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

## SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMB | * | =2x_DIELECTRIC | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

## HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| HDA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| HDA | * | =2x_DIELECTRIC | ? |
| MCP_HDA_COMP | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

## SIO Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_SLOW_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_SLOW | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

## SPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SPI | * | 8 MIL | ? |

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| MCP_DEBUG | PCI_55S | PCI | MCP_DEBUG<7..0> | 13 19 |
| PCI_AD | PCI_55S | PCI | PCI_AD<23..8> | |
| PCI_AD24 | PCI_55S | PCI | PCI_AD<24> | |
| PCI_AD | PCI_55S | PCI | PCI_AD<31..25> | |
| PCI_AD | PCI_55S | PCI | PCI_PAR | |
| PCI_C_BE_L | PCI_55S | PCI | PCI_C_BE_L<3..0> | |
| PCI_CNTL | PCI_55S | PCI | PCI_IRDY_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_DEVSEL_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_PERR_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_SERR_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_STOP_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_TRDY_L | |
| PCI_CNTL | PCI_55S | PCI | PCI_FRAME_L | |
| PCI_REQ0_L | PCI_55S | PCI | PCI_REQ0_L | 19 |
| PCI_GNT0_L | PCI_55S | PCI | PCI_GNT0_L | |
| PCI_REQ1_L | PCI_55S | PCI | PCI_REQ1_L | 19 |
| PCI_GNT1_L | PCI_55S | PCI | PCI_GNT1_L | |
| PCI_INTW_L | PCI_55S | PCI | PCI_INTW_L | |
| PCI_INTX_L | PCI_55S | PCI | PCI_INTX_L | |
| PCI_INTY_L | PCI_55S | PCI | PCI_INTY_L | |
| PCI_INTZ_L | PCI_55S | PCI | PCI_INTZ_L | |
| MCP_PCI_CLK2 | CLK_PCI_55S | CLK_PCI | PCI_CLK33M_MCP_R | 19 |
| | CLK_PCI_55S | CLK_PCI | PCI_CLK33M_MCP | 19 |
| LPC_AD | LPC_55S | LPC | LPC_AD<3..0> | 19 42 44 83 |
| LPC_FRAME_L | LPC_55S | LPC | LPC_FRAME_L | 19 42 44 83 |
| LPC_RESET_L | LPC_55S | LPC | LPC_RESET_L | 19 26 83 |
| MCP_LPC_CLK0 | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_SMC_R | 19 26 |
| | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_SMC | 26 42 |
| | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_LPCPLUS | 26 44 |
| USB_EXTA | USB_90D | USB | USB_EXTA_P | 20 40 |
| | USB_90D | USB | USB_EXTA_N | 20 40 |
| | USB_90D | USB | USB_EXTA_MUXED_P | |
| | USB_90D | USB | USB_EXTA_MUXED_N | |
| USB_MINI | USB_90D | USB | USB_MINI_P | 9 20 |
| | USB_90D | USB | USB_MINI_N | 9 20 |
| USB_EXTD | USB_90D | USB | USB_EXTD_P | 9 20 |
| | USB_90D | USB | USB_EXTD_N | 9 20 |
| USB_CAMERA | USB_90D | USB | USB_CAMERA_P | 20 31 |
| | USB_90D | USB | USB_CAMERA_N | 20 31 |
| USB_BT | USB_90D | USB | USB_BT_P | 20 31 |
| | USB_90D | USB | USB_BT_N | 20 31 |
| USB_TPAD | USB_90D | USB | USB_TPAD_P | 20 50 |
| | USB_90D | USB | USB_TPAD_N | 20 50 |
| USB_IR | USB_90D | USB | USB_IR_P | 20 41 |
| | USB_90D | USB | USB_IR_N | 20 41 |
| USB_EXTB | USB_90D | USB | USB_EXTB_P | 20 40 |
| | USB_90D | USB | USB_EXTB_N | 20 40 |
| USB_EXCARD | USB_90D | USB | USB_EXCARD_P | 20 32 |
| | USB_90D | USB | USB_EXCARD_N | 20 32 |
| USB_EXTC | USB_90D | USB | USB_EXTC_P | 9 20 |
| | USB_90D | USB | USB_EXTC_N | 9 20 |
| MCP_USB_RBIAS | MCP_USB_RBIAS | | MCP_USB_RBIAS_GND | 20 |
| SMBUS_MCP_0_CLK | SMB_55S | SMB | SMBUS_MCP_0_CLK | 7 13 21 45 |
| SMBUS_MCP_0_DATA | SMB_55S | SMB | SMBUS_MCP_0_DATA | 7 13 21 45 |
| SMBUS_MCP_1_CLK | SMB_55S | SMB | SMBUS_MCP_1_CLK | 21 45 |
| SMBUS_MCP_1_DATA | SMB_55S | SMB | SMBUS_MCP_1_DATA | 21 45 |
| HDA_BIT_CLK | HDA_55S | HDA | HDA_BIT_CLK | 9 21 |
| | HDA_55S | HDA | HDA_BIT_CLK_R | 21 |
| HDA_SYNC | HDA_55S | HDA | HDA_SYNC | 21 54 |
| | HDA_55S | HDA | HDA_SYNC_R | 21 |
| HDA_RST_L | HDA_55S | HDA | HDA_RST_R_L | 21 |
| | HDA_55S | HDA | HDA_RST_L | 21 54 |
| HDA_SDIN0 | HDA_55S | HDA | HDA_SDIN0 | 21 54 |
| | HDA_55S | HDA | HDA_SDIN_CODEC | |
| HDA_SDOUT | HDA_55S | HDA | HDA_SDOUT | 21 54 |
| | HDA_55S | HDA | HDA_SDOUT_R | 21 |
| MCP_HDA_PULLDN_COMP | | MCP_HDA_COMP | MCP_HDA_PULLDN_COMP | 21 |
| MCP_SUS_CLK | CLK_SLOW_55S | CLK_SLOW | PM_CLK32K_SUSCLK_R | 21 26 |
| | CLK_SLOW_55S | CLK_SLOW | PM_CLK32K_SUSCLK | 26 42 |
| SPI_CLK | SPI_55S | SPI | SPI_CLK_R | 21 44 |
| | SPI_55S | SPI | SPI_CLK | 44 53 |
| SPI_MOSI | SPI_55S | SPI | SPI_MOSI_R | 21 44 |
| | SPI_55S | SPI | SPI_MOSI | 44 53 |
| SPI_MISO | SPI_55S | SPI | SPI_MISO | 21 44 |
| | SPI_55S | SPI | SPI_MISO_R | 53 |
| SPI_CS0 | SPI_55S | SPI | SPI_CS0_R_L | 21 44 |
| | SPI_55S | SPI | SPI_CS0_L | |

# MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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| SCALE | SHT | OF |
|---|---|---|
| NONE | 103 | 109 |

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# MCP RGMII (Ethernet) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MCP_MII_COMP | * | =STANDARD | 7.5 MIL | 7.5 MIL | =STANDARD | =STANDARD | =STANDARD |
| ENET_MII_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MCP_BUF0_CLK | * | =3:1_SPACING | ? |
| ENET_MII | * | 12 MIL | ? |

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

# 88E1116R (Ethernet PHY) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| ENET_MDI_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENET_MDI | * | 25 MIL | ? |

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| MCP_MII_COMP | MCP_MII_COMP | | MCP_MII_COMP_VDD | 18 |
| MCP_MII_COMP | MCP_MII_COMP | | MCP_MII_COMP_GND | 18 |
| MCP_CLK25M_BUF0 | ENET_MII_55S | MCP_BUF0_CLK | MCP_CLK25M_BUF0_R | 18 34 |
| | ENET_MII_55S | MCP_BUF0_CLK | RTL8211_CLK25M_CKXTAL1 | 33 34 |
| ENET_INTR_L | ENET_MII_55S | ENET_MII | ENET_INTR_L | |
| ENET_MDIO | ENET_MII_55S | ENET_MII | ENET_MDIO | 18 33 |
| ENET_MDC | ENET_MII_55S | ENET_MII | ENET_MDC | 18 33 |
| ENET_PWRDWN_L | ENET_MII_55S | ENET_MII | ENET_PWRDWN_L | |
| | ENET_MII_55S | ENET_MII | ENET_CLK125M_RXCLK_R | 33 |
| ENET_RXCLK | ENET_MII_55S | ENET_MII | ENET_CLK125M_RXCLK | 18 33 |
| | ENET_MII_55S | ENET_MII | ENET_RXD_R<3..0> | 33 |
| ENET_RXD | ENET_MII_55S | ENET_MII | ENET_RXD<0> | 18 33 |
| ENET_RXD_STRAP | ENET_MII_55S | ENET_MII | ENET_RXD<3..1> | 18 33 |
| ENET_RXD | ENET_MII_55S | ENET_MII | ENET_RX_CTRL | 18 33 |
| ENET_TXCLK | ENET_MII_55S | ENET_MII | ENET_CLK125M_TXCLK | 18 33 |
| ENET_TXD0 | ENET_MII_55S | ENET_MII | ENET_TXD<0> | 18 33 |
| ENET_TXD | ENET_MII_55S | ENET_MII | ENET_TXD<3..1> | 18 33 |
| ENET_TXD | ENET_MII_55S | ENET_MII | ENET_TX_CTRL | 18 33 |
| | ENET_MII_55S | ENET_MII | ENET_RESET_L | 18 33 |
| ENET_MDI | ENET_MDI_100D | ENET_MDI | ENET_MDI_P<3..0> | 33 35 |
| | ENET_MDI_100D | ENET_MDI | ENET_MDI_N<3..0> | 33 35 |

# Ethernet Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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# FireWire Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| FW_110D | * | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| FW_TP | * | =3:1_SPACING | ? |

# FireWire Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING |
|---|---|---|
| FW_P0_TPA | FW_110D | FW_TP |
| FW_P0_TPA | FW_110D | FW_TP |
| FW_P0_TPB | FW_110D | FW_TP |
| FW_P0_TPB | FW_110D | FW_TP |
| FW_P1_TPA | FW_110D | FW_TP |
| FW_P1_TPA | FW_110D | FW_TP |
| FW_P1_TPB | FW_110D | FW_TP |
| FW_P1_TPB | FW_110D | FW_TP |
| Port 2 Not Used | | |

FW_P0_TPA_P 36 38
FW_P0_TPA_N 36 38
FW_P0_TPB_P 36 38
FW_P0_TPB_N 36 38
FW_P1_TPA_P 36 38
FW_P1_TPA_N 36 38
FW_P1_TPB_P 36 38
FW_P1_TPB_N 36 38

FireWire Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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|---|---|---|
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| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 1TO1_DIFFPAIR | * | =STANDARD | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.1 MM |

## SMC SMBus Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | SPACING | |
|---|---|---|---|
| SMBUS_SMC_A_S3_SCL | SMB_55S | SMB | SMBUS_SMC_A_S3_SCL 7 45 |
| SMBUS_SMC_A_S3_SDA | SMB_55S | SMB | SMBUS_SMC_A_S3_SDA 7 45 |
| SMBUS_SMC_B_S0_SCL | SMB_55S | SMB | SMBUS_SMC_B_S0_SCL 45 |
| SMBUS_SMC_B_S0_SDA | SMB_55S | SMB | SMBUS_SMC_B_S0_SDA 45 |
| SMBUS_SMC_0_S0_SCL | SMB_55S | SMB | SMBUS_SMC_0_S0_SCL 45 |
| SMBUS_SMC_0_S0_SDA | SMB_55S | SMB | SMBUS_SMC_0_S0_SDA 45 |
| SMBUS_SMC_BSA_SCL | SMB_55S | SMB | SMBUS_SMC_BSA_SCL 45 |
| SMBUS_SMC_BSA_SDA | SMB_55S | SMB | SMBUS_SMC_BSA_SDA 45 |
| SMBUS_SMC_MGMT_SCL | SMB_55S | SMB | SMBUS_SMC_MGMT_SCL 45 |
| SMBUS_SMC_MGMT_SDA | SMB_55S | SMB | SMBUS_SMC_MGMT_SDA 45 |

## SMBus Charger Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | SPACING | |
|---|---|---|---|
| CHGR_CSI | 1TO1_DIFFPAIR | | CHGR_CSI_P 61 |
| | 1TO1_DIFFPAIR | | CHGR_CSI_N 61 |
| CHGR_CSO | 1TO1_DIFFPAIR | | CHGR_CSO_P 61 |
| | 1TO1_DIFFPAIR | | CHGR_CSO_N 61 |

# SMC Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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## GDDR3 Frame Buffer Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| GDDR3_40R55SE | * | =55_OHM_SE | =40_OHM_SE | 0.095 MM | 12.7 MM | =STANDARD | =STANDARD |
| GDDR3_40SE | * | =40_OHM_SE | =40_OHM_SE | 0.095 MM | =40_OHM_SE | =STANDARD | =STANDARD |
| GDDR3_80D | * | =80_OHM_DIFF | =80_OHM_DIFF | 0.095 MM | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GDDR3_CLK | * | =2.5:1_SPACING | ? |
| GDDR3_CMD | * | =2.5:1_SPACING | ? |
| GDDR3_DATA | * | =2.5:1_SPACING | ? |
| GDDR3_DQS | * | =2.5:1_SPACING | ? |

## From T18 MXM:
## Digital Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DP_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| LVDS_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | * | =3x_DIELECTRIC | ? |
| LVDS | * | =3x_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| LVDS | TOP,BOTTOM | =4x_DIELECTRIC | ? |

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

## MUXGFX Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| LVDS_A_CLK | LVDS_100D | LVDS | LVDS_A_CLK_P | 80 83 |
| LVDS_A_CLK | LVDS_100D | LVDS | LVDS_A_CLK_N | 80 83 |
| LVDS_A_DATA | LVDS_100D | LVDS | LVDS_A_DATA_P<2..0> | 80 83 |
| LVDS_A_DATA | LVDS_100D | LVDS | LVDS_A_DATA_N<2..0> | 80 83 |
| LVDS_B_CLK | LVDS_100D | LVDS | LVDS_B_CLK_P | 80 83 |
| LVDS_B_CLK | LVDS_100D | LVDS | LVDS_B_CLK_N | 80 83 |
| LVDS_B_DATA | LVDS_100D | LVDS | LVDS_B_DATA_P<2..0> | 80 83 |
| LVDS_B_DATA | LVDS_100D | LVDS | LVDS_B_DATA_N<2..0> | 80 83 |
| | LVDS_100D | LVDS | LVDS_CONN_A_CLK_F_P | 7 79 |
| | LVDS_100D | LVDS | LVDS_CONN_A_CLK_F_N | 7 79 |
| | LVDS_100D | LVDS | LVDS_CONN_B_CLK_F_P | 7 79 |
| | LVDS_100D | LVDS | LVDS_CONN_B_CLK_F_N | 7 79 |
| | LVDS_100D | LVDS | LVDS_CONN_A_CLK_P | 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_A_CLK_N | 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_A_DATA_P<2..0> | 7 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_A_DATA_N<2..0> | 7 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_B_CLK_P | 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_B_CLK_N | 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_B_DATA_P<2..0> | 7 79 80 |
| | LVDS_100D | LVDS | LVDS_CONN_B_DATA_N<2..0> | 7 79 80 |
| DP_ML | DP_100D | DISPLAYPORT | DP_ML_C_P<3..0> | 81 |
| DP_ML | DP_100D | DISPLAYPORT | DP_ML_C_N<3..0> | 81 |
| DP_ML | DP_100D | DISPLAYPORT | **DP_ML_P<3..0>** | 80 81 |
| DP_ML | DP_100D | DISPLAYPORT | **DP_ML_N<3..0>** | 80 81 |
| DP_ML | DP_100D | DISPLAYPORT | DP_ML_CONN_P<3..0> | 81 |
| DP_ML | DP_100D | DISPLAYPORT | DP_ML_CONN_N<3..0> | 81 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_AUX_CH_C_P | 80 81 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_AUX_CH_C_N | 80 81 |

## GDDR3 FB A/B Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| FB_A_CLK_P | GDDR3_80D | GDDR3_CLK | FB_A_CLK_P<0> | 72 73 |
| | GDDR3_80D | GDDR3_CLK | FB_A_CLK_N<0> | 72 73 |
| FB_B_CLK_P | GDDR3_80D | GDDR3_CLK | FB_A_CLK_P<1> | 72 73 |
| | GDDR3_80D | GDDR3_CLK | FB_A_CLK_N<1> | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_MA<1..0> | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_MA<12..6> | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_BA<2..0> | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_RAS_L | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_CAS_L | 72 73 |
| FB_AB_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_A_WE_L | 72 73 |
| FB_AB_CMD_PD | GDDR3_40R55SE | GDDR3_CMD | FB_A_CKE | 72 73 |
| FB_AB_CS0 | GDDR3_40R55SE | GDDR3_CMD | FB_A_CS0_L | 72 73 |
| FB_AB_CMD_PD | GDDR3_40R55SE | GDDR3_CMD | FB_A_DRAM_RST | 72 73 |
| FB_A_CMD | GDDR3_40SE | GDDR3_CMD | FB_A_LMA<5..2> | 72 73 |
| FB_B_CMD | GDDR3_40SE | GDDR3_CMD | FB_A_UMA<5..2> | 72 73 |
| FB_A_WDQS0 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<0> | 72 73 |
| FB_A_WDQS1 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<1> | 72 73 |
| FB_A_WDQS2 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<2> | 72 73 |
| FB_A_WDQS3 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<3> | 72 73 |
| FB_A_RDQS0 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<0> | 72 73 |
| FB_A_RDQS1 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<1> | 72 73 |
| FB_A_RDQS2 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<2> | 72 73 |
| FB_A_RDQS3 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<3> | 72 73 |
| FB_A_DQ_BYTE0 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<7..0> | 72 73 |
| FB_A_DQ_BYTE1 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<15..8> | 72 73 |
| FB_A_DQ_BYTE2 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<23..16> | 72 73 |
| FB_A_DQ_BYTE3 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<31..24> | 72 73 |
| FB_A_DQM0 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<0> | 72 73 |
| FB_A_DQM1 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<1> | 72 73 |
| FB_A_DQM2 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<2> | 72 73 |
| FB_A_DQM3 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<3> | 72 73 |
| FB_B_WDQS0 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<4> | 72 73 |
| FB_B_WDQS1 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<5> | 72 73 |
| FB_B_WDQS2 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<6> | 72 73 |
| FB_B_WDQS3 | GDDR3_40SE | GDDR3_DQS | FB_A_WDQS<7> | 72 73 |
| FB_B_RDQS0 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<4> | 72 73 |
| FB_B_RDQS1 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<5> | 72 73 |
| FB_B_RDQS2 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<6> | 72 73 |
| FB_B_RDQS3 | GDDR3_40SE | GDDR3_DQS | FB_A_RDQS<7> | 72 73 |
| FB_B_DQ_BYTE0 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<39..32> | 72 73 |
| FB_B_DQ_BYTE1 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<47..40> | 72 73 |
| FB_B_DQ_BYTE2 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<55..48> | 72 73 |
| FB_B_DQ_BYTE3 | GDDR3_40SE | GDDR3_DATA | FB_A_DQ<63..56> | 72 73 |
| FB_B_DQM0 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<4> | 72 73 |
| FB_B_DQM1 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<5> | 72 73 |
| FB_B_DQM2 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<6> | 72 73 |
| FB_B_DQM3 | GDDR3_40SE | GDDR3_DATA | FB_A_DQM_L<7> | 72 73 |

## G96 Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| (CK505_DOT96) | CLK_SLOW_555 | CLK_SLOW | GPU_CLK27M | 76 |
| CK505_CLK27M55 | CLK_SLOW_555 | CLK_SLOW | GPU_CLK27M_SS | 76 |
| LVDS_EG_A_CLK | LVDS_100D | LVDS | LVDS_EG_A_CLK_P | 77 83 |
| LVDS_EG_A_CLK | LVDS_100D | LVDS | LVDS_EG_A_CLK_N | 77 83 |
| LVDS_EG_A_DATA | LVDS_100D | LVDS | LVDS_EG_A_DATA_P<2..0> | 77 83 |
| LVDS_EG_A_DATA | LVDS_100D | LVDS | LVDS_EG_A_DATA_N<2..0> | 77 83 |
| LVDS_EG_B_DATA | LVDS_100D | LVDS | LVDS_EG_B_DATA_P<2..0> | 77 83 |
| LVDS_EG_B_DATA | LVDS_100D | LVDS | LVDS_EG_B_DATA_N<2..0> | 77 83 |
| DP_ML | DP_100D | DISPLAYPORT | **DP_EG_ML_P<3..0>** | 77 80 |
| DP_ML | DP_100D | DISPLAYPORT | **DP_EG_ML_N<3..0>** | 77 80 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_EG_AUX_CH_P | 77 80 |
| DP_AUX_CH | DP_100D | DISPLAYPORT | DP_EG_AUX_CH_N | 77 80 |
| | DP_100D | DISPLAYPORT | DP_EG_AUX_CH_C_P | 80 |
| | DP_100D | DISPLAYPORT | DP_EG_AUX_CH_C_N | 80 |

## GDDR3 FB C/D Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| FB_C_CLK_P | GDDR3_80D | GDDR3_CLK | FB_B_CLK_P<0> | 72 74 |
| | GDDR3_80D | GDDR3_CLK | FB_B_CLK_N<0> | 72 74 |
| FB_D_CLK_P | GDDR3_80D | GDDR3_CLK | FB_B_CLK_P<1> | 72 74 |
| | GDDR3_80D | GDDR3_CLK | FB_B_CLK_N<1> | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_MA<1..0> | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_MA<12..6> | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_BA<2..0> | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_RAS_L | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_CAS_L | 72 74 |
| FB_CD_CMD | GDDR3_40R55SE | GDDR3_CMD | FB_B_WE_L | 72 74 |
| FB_CD_CMD_PD | GDDR3_40R55SE | GDDR3_CMD | FB_B_CKE | 72 74 |
| FB_CD_CS0 | GDDR3_40R55SE | GDDR3_CMD | FB_B_CS0_L | 72 74 |
| FB_CD_CMD_PD | GDDR3_40R55SE | GDDR3_CMD | FB_B_DRAM_RST | 72 74 |
| FB_C_CMD | GDDR3_40SE | GDDR3_CMD | FB_B_LMA<5..2> | 72 74 |
| FB_D_CMD | GDDR3_40SE | GDDR3_CMD | FB_B_UMA<5..2> | 72 74 |
| FB_C_WDQS0 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<0> | 72 74 |
| FB_C_WDQS1 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<1> | 72 74 |
| FB_C_WDQS2 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<2> | 72 74 |
| FB_C_WDQS3 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<3> | 72 74 |
| FB_C_RDQS0 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<0> | 72 74 |
| FB_C_RDQS1 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<1> | 72 74 |
| FB_C_RDQS2 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<2> | 72 74 |
| FB_C_RDQS3 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<3> | 72 74 |
| FB_C_DQ_BYTE0 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<7..0> | 72 74 |
| FB_C_DQ_BYTE1 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<15..8> | 72 74 |
| FB_C_DQ_BYTE2 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<23..16> | 72 74 |
| FB_C_DQ_BYTE3 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<31..24> | 72 74 |
| FB_C_DQM0 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<0> | 72 74 |
| FB_C_DQM1 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<1> | 72 74 |
| FB_C_DQM2 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<2> | 72 74 |
| FB_C_DQM3 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<3> | 72 74 |
| FB_D_WDQS0 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<4> | 72 74 |
| FB_D_WDQS1 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<5> | 72 74 |
| FB_D_WDQS2 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<6> | 72 74 |
| FB_D_WDQS3 | GDDR3_40SE | GDDR3_DQS | FB_B_WDQS<7> | 72 74 |
| FB_D_RDQS0 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<4> | 72 74 |
| FB_D_RDQS1 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<5> | 72 74 |
| FB_D_RDQS2 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<6> | 72 74 |
| FB_D_RDQS3 | GDDR3_40SE | GDDR3_DQS | FB_B_RDQS<7> | 72 74 |
| FB_D_DQ_BYTE0 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<39..32> | 72 74 |
| FB_D_DQ_BYTE1 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<47..40> | 72 74 |
| FB_D_DQ_BYTE2 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<55..48> | 72 74 |
| FB_D_DQ_BYTE3 | GDDR3_40SE | GDDR3_DATA | FB_B_DQ<63..56> | 72 74 |
| FB_D_DQM0 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<4> | 72 74 |
| FB_D_DQM1 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<5> | 72 74 |
| FB_D_DQM2 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<6> | 72 74 |
| FB_D_DQM3 | GDDR3_40SE | GDDR3_DATA | FB_B_DQM_L<7> | 72 74 |

## GPU (G96) Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008


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| D | 051-7902 | D |

SCALE: NONE SHT: 107 OF: 109

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| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SENSE_1TO1_55S | * | =1:1_DIFFPAIR | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |
| THERM_1TO1_55S | * | =1:1_DIFFPAIR | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |
| DIFFPAIR | * | =1:1_DIFFPAIR | | | =1:1_DIFFPAIR | =1:1_DIFFPAIR | =1:1_DIFFPAIR |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SENSE | * | =2:1_SPACING | ? |
| THERM | * | =2:1_SPACING | ? |
| AUDIO | * | =2:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENETCONN | * | 25 MILS | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GND | * | =STANDARD | ? |
| PP1V8_MEM | * | =STANDARD | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GND_P2MM | * | 0.20 MM | 1000 |
| PWR_P2MM | * | 0.20 MM | 1000 |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CLK | GND | * | GND_P2MM |
| MEM_CMD | GND | * | GND_P2MM |
| MEM_CTRL | GND | * | GND_P2MM |
| MEM_DATA | GND | * | GND_P2MM |
| MEM_DQS | GND | * | GND_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_PCIE | GND | * | GND_P2MM |
| PCIE | GND | * | GND_P2MM |
| SATA | GND | * | GND_P2MM |
| USB | GND | * | GND_P2MM |
| CLK_PCIE | SB_POWER | * | PWR_P2MM |
| SATA | SB_POWER | * | PWR_P2MM |
| USB | SB_POWER | * | PWR_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_FSB | GND | * | GND_P2MM |
| CPU_COMP | GND | * | GND_P2MM |
| CPU_GTLREF | GND | * | GND_P2MM |
| CPU_VCCSENSE | GND | * | GND_P2MM |
| FSB_DSTB | FSB_DSTB | * | GND_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| ENET_MDI | GND | * | GND_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| LVDS | GND | * | GND_P2MM |

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_70D | BOTTOM | | | 0.127 MM | 6.35 MM | | |

## Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| LVDS_100D | BGA | 100_DIFF_BGA |
| DP_100D | BGA | 100_DIFF_BGA |
| SATA_100D | BGA | 100_DIFF_BGA |

## M99 Specific Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | ENET_MDI_100D | ENETCONN | ENETCONN_P<3..0> | 35 |
| | ENET_MDI_100D | ENETCONN | ENETCONN_N<3..0> | 35 |
| U14G | SATA_100D | SATA | SATA_ODD_R2D_UF_P | 39 |
| U14F | SATA_100D | SATA | SATA_ODD_R2D_UF_N | 39 |
| U14J | SATA_100D | SATA | SATA_ODD_D2R_UF_P | 39 |
| U14H | SATA_100D | SATA | SATA_ODD_D2R_UF_N | 39 |
| U14L | SATA_100D | SATA | SATA_HDD_D2R_UF_P | 39 |
| U14K | SATA_100D | SATA | SATA_HDD_D2R_UF_N | 39 |
| U14M | SATA_100D | SATA | SATA_HDD_R2D_UF_P | 39 |
| U13P | SATA_100D | SATA | SATA_HDD_R2D_UF_N | 39 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | GFXIMVP6_VSEN_P | 78 |
| | SENSE_1TO1_55S | SENSE | GFXIMVP6_VSEN_N | 78 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | MCPCOREISNS_P | 47 65 |
| | SENSE_1TO1_55S | SENSE | MCPCOREISNS_N | 47 65 |
| CPUTHMSNS_D2_DP | THERM_1TO1_55S | THERM | CPUTHMSNS_D2_P | 48 |
| U12S | THERM_1TO1_55S | THERM | CPUTHMSNS_D2_N | 48 |
| CPU_THERMD_DP | THERM_1TO1_55S | THERM | CPU_THERMD_P | 10 48 |
| U12G | THERM_1TO1_55S | THERM | CPU_THERMD_N | 10 48 |
| GPUTHMSNS_D_DP | THERM_1TO1_55S | THERM | GPUTHMSNS_D_P | 48 |
| U13S | THERM_1TO1_55S | THERM | GPUTHMSNS_D_N | 48 |
| GPU_THERMD_DP | THERM_1TO1_55S | THERM | GPU_TDIODE_P | 48 76 |
| U12F | THERM_1TO1_55S | THERM | GPU_TDIODE_N | 48 76 |
| MCPTHMSNS_D_DP | THERM_1TO1_55S | THERM | MCPTHMSNS_D_P | 48 |
| U13R | THERM_1TO1_55S | THERM | MCPTHMSNS_D_N | 48 |
| MCP_THERMD_DP | THERM_1TO1_55S | THERM | MCP_THMDIODE_P | 21 48 |
| U13G | THERM_1TO1_55S | THERM | MCP_THMDIODE_N | 21 48 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | 1V05CPUISNS_R_P | 47 |
| U15T | SENSE_1TO1_55S | SENSE | 1V05CPUISNS_R_N | 47 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | DDRISNS_R_P | 47 |
| U15S | SENSE_1TO1_55S | SENSE | DDRISNS_R_N | 47 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | GPUISENS_P | 47 |
| U15J | SENSE_1TO1_55S | SENSE | GPUISENS_N | 47 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | 1V05CPU_P | 47 66 |
| U15U | SENSE_1TO1_55S | SENSE | 1V05CPU_N | 47 66 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | DDRISNS_P | 47 |
| U14P | SENSE_1TO1_55S | SENSE | DDRISNS_N | 47 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | P1V8GPU_P | 47 |
| U14T | SENSE_1TO1_55S | SENSE | P1V8GPU_N | 47 |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | ISNS_CPU_P | 46 |
| U16P | SENSE_1TO1_55S | SENSE | ISNS_CPU_N | 46 |
| U16R | | GND | GND | |
| | | SB_POWER | PP3V3_S5 | 7 8 |
| | | SB_POWER | PP3V3_S0 | 7 8 |
| | | SB_POWER | PP1V5_S0 | |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | P1V8GPUISNS_P | |
| U15P | SENSE_1TO1_55S | SENSE | P1V8GPUISNS_N | |
| SENSE_DIFFPAIR | SENSE_1TO1_55S | SENSE | P1V8GPUISNS_R_P | 47 |
| U15R | SENSE_1TO1_55S | SENSE | P1V8GPUISNS_R_N | 47 |

## M99 Specific Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| U16G (PCIE_EXCARD) | PCIE_90D | PCIE | PCIE_EXCARD_R2D_P | 7 32 89 |
| U16F (PCIE_EXCARD) | PCIE_90D | PCIE | PCIE_EXCARD_R2D_N | 7 32 89 |
| U16J (PCIE_MINI) | PCIE_90D | PCIE | PCIE_MINI_R2D_P | 31 89 |
| U16H (PCIE_MINI) | PCIE_90D | PCIE | PCIE_MINI_R2D_N | 31 89 |
| U16D | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_CONN_P | 31 |
| U16C | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_CONN_N | 31 |
| U16K | 1TO1_DIFFPAIR | | CHGR_CSI_R_P | 61 |
| U16L | 1TO1_DIFFPAIR | | CHGR_CSI_R_N | 61 |
| U16N | 1TO1_DIFFPAIR | | CHGR_CSO_R_P | 46 61 |
| U16M | 1TO1_DIFFPAIR | | CHGR_CSO_R_N | 46 61 |
| U18P (USB_EXTA) | USB_90D | USB | USB2_EXTA_MUXED_P | 40 |
| U18N (USB_EXTA) | USB_90D | USB | USB2_EXTA_MUXED_N | 40 |
| U17P (USB_EXTA) | USB_90D | USB | USB2_LT1_P | 40 |
| U18R (USB_EXTA) | USB_90D | USB | USB2_LT1_N | 40 |
| U17J (USB_EXTD) | USB_90D | USB | CONN_TPAD_USB_P | |
| U17H (USB_EXTD) | USB_90D | USB | CONN_TPAD_USB_N | |
| U17G (USB_CAMERA) | USB_90D | USB | USB_CAMERA_CONN_P | 31 |
| U17F (USB_CAMERA) | USB_90D | USB | USB_CAMERA_CONN_N | 31 |
| U17K | USB_90D | USB | CONN_USB2_BT_P | 31 |
| U17L | USB_90D | USB | CONN_USB2_BT_N | 31 |
| U17M | USB_90D | USB | USB_LT2_P | 40 |
| U17N | USB_90D | USB | USB_LT2_N | 40 |
| U16G | USB_90D | USB | USB2_EXCARD_CONN_P | 7 32 |
| U17C | USB_90D | USB | USB2_EXCARD_CONN_N | 7 32 |
| U18K | DP_100D | DISPLAYPORT | DP_IG_AUX_CH_C_P | 80 |
| U18L | DP_100D | DISPLAYPORT | DP_IG_AUX_CH_C_N | 80 |
| U18F MCP_PE4_REFCLK | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_FC_P | 9 32 |
| U18G | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_FC_N | 9 32 |
| U18B PCIE_FC_R2D | PCIE_90D | PCIE | PCIE_FC_R2D_C_P | 9 32 |
| U18C | PCIE_90D | PCIE | PCIE_FC_R2D_C_N | 9 32 |
| U18A PCIE_FC_D2R | PCIE_90D | PCIE | PCIE_FC_D2R_P | 9 32 |
| U18D | PCIE_90D | PCIE | PCIE_FC_D2R_N | 9 32 |
| U18J | PCIE_90D | PCIE | PCIE_FC_R2D_P | 32 |
| U18H | PCIE_90D | PCIE | PCIE_FC_R2D_N | 32 |
| U16E | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_CONN_N | 7 32 |
| U16D | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_CONN_P | 7 32 |
| U19D SPK_OUT | DIFFPAIR | AUDIO | SPKRCONN_L_P_OUT | 7 57 58 |
| U19C | DIFFPAIR | AUDIO | SPKRCONN_L_N_OUT | 7 57 58 |
| U20D SPK_OUT | DIFFPAIR | AUDIO | SPKRCONN_S_P_OUT | 7 57 58 |
| U20C | DIFFPAIR | AUDIO | SPKRCONN_S_N_OUT | 7 57 58 |
| U19B SPK_OUT | DIFFPAIR | AUDIO | SPKRCONN_R_P_OUT | 7 57 58 |
| U19A | DIFFPAIR | AUDIO | SPKRCONN_R_N_OUT | 7 57 58 |
| U20B | DIFFPAIR | AUDIO | SPKRAMP_L_P_OUT | 57 |
| U20A | DIFFPAIR | AUDIO | SPKRAMP_L_N_OUT | 57 |
| U26D | DIFFPAIR | AUDIO | SPKRAMP_R_P_OUT | 57 |
| U26C | DIFFPAIR | AUDIO | SPKRAMP_R_N_OUT | 57 |
| U26B | DIFFPAIR | AUDIO | SPKRAMP_S_P_OUT | 57 |
| U26A | DIFFPAIR | AUDIO | SPKRAMP_S_N_OUT | 57 |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_40S OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 5.8 MM OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_40S_VDD OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 5.8 MM OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_70D OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 5.8 MM OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_70D_VDD OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| PCIE_90D OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| USB_90D OVERRIDE | TOP OVERRIDE | OVERRIDE | OVERRIDE | 0.09 MM OVERRIDE | 500 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MCP_DV_COMP OVERRIDE | TOP OVERRIDE | OVERRIDE | OVERRIDE | 0.1 MM OVERRIDE | 500 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MCP_MEM_COMP OVERRIDE | TOP OVERRIDE | OVERRIDE | OVERRIDE | 0.1 MM OVERRIDE | 500 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MCP_MII_COMP OVERRIDE | TOP OVERRIDE | OVERRIDE | OVERRIDE | 0.1 MM OVERRIDE | 500 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MCP_USB_RBIAS OVERRIDE | TOP OVERRIDE | OVERRIDE | OVERRIDE | 0.1 MM OVERRIDE | 500 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MCP_DV_COMP OVERRIDE | * OVERRIDE | OVERRIDE | OVERRIDE | 0.25 MM OVERRIDE | 250 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| CPU_27P4S OVERRIDE | BOTTOM OVERRIDE | OVERRIDE | OVERRIDE | 0.23 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_40S OVERRIDE | ISL4,ISL9 OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_40S_VDD OVERRIDE | ISL3,ISL10 OVERRIDE | N OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_70D OVERRIDE | ISL4,ISL9 OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_70D_VDD OVERRIDE | ISL3,ISL10 OVERRIDE | N OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE | OVERRIDE |

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

## Project Specific Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/21/2008


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| D | 051-7902 | D |
| SCALE: NONE | SHT 108 OF 109 | |

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# M99 Board-Specific Spacing & Physical Constraints

| BOARD LAYERS | BOARD AREAS | BOARD UNITS (MIL or MM) | ALLEGRO VERSION |
|---|---|---|---|
| TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM | NO_TYPE,BGA | MM | 15.5.1 |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DEFAULT | * | Y | =50_OHM_SE | =50_OHM_SE | 14 MM | 0 MM | 0 MM |
| STANDARD | * | Y | =DEFAULT | =DEFAULT | 10 MM | =DEFAULT | =DEFAULT |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 55_OHM_SE | TOP,BOTTOM | Y | 0.090 MM | 0.090 MM | | | |
| 55_OHM_SE | * | Y | 0.076 MM | 0.076 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 50_OHM_SE | TOP,BOTTOM | Y | 0.110 MM | 0.095 MM | | | |
| 50_OHM_SE | * | Y | 0.090 MM | 0.090 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 40_OHM_SE | TOP,BOTTOM | Y | 0.165 MM | 0.095 MM | | | |
| 40_OHM_SE | * | Y | 0.135 MM | 0.135 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 27P4_OHM_SE | TOP,BOTTOM | Y | 0.310 MM | 0.095 MM | | | |
| 27P4_OHM_SE | * | Y | 0.250 MM | 0.250 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 70_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 70_OHM_DIFF | ISL3,ISL4 | Y | 0.160 MM | 0.160 MM | | 0.175 MM | 0.175 MM |
| 70_OHM_DIFF | ISL9,ISL10 | Y | 0.160 MM | 0.160 MM | | 0.175 MM | 0.175 MM |
| 70_OHM_DIFF | ISL2,ISL11 | Y | 0.170 MM | 0.170 MM | | 0.150 MM | 0.150 MM |
| 70_OHM_DIFF | TOP,BOTTOM | Y | 0.170 MM | 0.095 MM | | 0.150 MM | 0.150 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 80_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 80_OHM_DIFF | ISL3,ISL4 | Y | 0.125 MM | 0.125 MM | | 0.180 MM | 0.180 MM |
| 80_OHM_DIFF | ISL9,ISL10 | Y | 0.125 MM | 0.125 MM | | 0.180 MM | 0.180 MM |
| 80_OHM_DIFF | ISL2,ISL11 | Y | 0.140 MM | 0.140 MM | | 0.190 MM | 0.190 MM |
| 80_OHM_DIFF | TOP,BOTTOM | Y | 0.140 MM | 0.095 MM | | 0.190 MM | 0.190 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 90_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 90_OHM_DIFF | ISL3,ISL4 | Y | 0.102 MM | 0.102 MM | | 0.220 MM | 0.220 MM |
| 90_OHM_DIFF | ISL9,ISL10 | Y | 0.102 MM | 0.102 MM | | 0.220 MM | 0.220 MM |
| 90_OHM_DIFF | ISL2,ISL11 | Y | 0.115 MM | 0.115 MM | | 0.230 MM | 0.230 MM |
| 90_OHM_DIFF | TOP,BOTTOM | Y | 0.115 MM | 0.095 MM | | 0.230 MM | 0.230 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 100_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 100_OHM_DIFF | ISL3,ISL4 | Y | 0.080 MM | 0.080 MM | | 0.200 MM | 0.200 MM |
| 100_OHM_DIFF | ISL9,ISL10 | Y | 0.080 MM | 0.080 MM | | 0.200 MM | 0.200 MM |
| 100_OHM_DIFF | ISL2,ISL11 | Y | 0.089 MM | 0.089 MM | | 0.220 MM | 0.220 MM |
| 100_OHM_DIFF | TOP,BOTTOM | Y | 0.089 MM | 0.089 MM | | 0.220 MM | 0.220 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 110_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 110_OHM_DIFF | ISL3,ISL4 | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | ISL9,ISL10 | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | ISL2,ISL11 | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | TOP,BOTTOM | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DEFAULT | * | 0.1 MM | ? |
| STANDARD | * | =DEFAULT | ? |
| BGA_P1MM | * | =DEFAULT | ? |
| BGA_P2MM | * | =DEFAULT | ? |
| BGA_P3MM | * | =DEFAULT | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 1.5:1_SPACING | * | 0.15 MM | ? |
| 1.8:1_SPACING | * | 0.18 MM | ? |
| 2:1_SPACING | * | 0.2 MM | ? |
| 2.5:1_SPACING | * | 0.25 MM | ? |
| 3:1_SPACING | * | 0.3 MM | ? |
| 4:1_SPACING | * | 0.4 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| * | * | BGA | BGA_P1MM |
| MEM_CLK | * | BGA | BGA_P2MM |
| CLK_FSB | * | BGA | BGA_P2MM |
| CLK_PCIE | * | BGA | BGA_P2MM |
| CLK_SLOW | * | BGA | BGA_P2MM |
| FSB_DSTB | FSB_DSTB | BGA | BGA_P3MM |

NOTE:From T18 MLB, changed to reflect M99 stackup.

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 2X_DIELECTRIC | * | 0.140 MM | ? |
| 3X_DIELECTRIC | * | 0.210 MM | ? |
| 4X_DIELECTRIC | * | 0.280 MM | ? |
| 5X_DIELECTRIC | * | 0.350 MM | ? |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 1:1_DIFFPAIR | * | Y | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 100_DIFF_BGA | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| 100_DIFF_BGA | ISL3,ISL4 | Y | 0.075 MM | 0.075 MM | | 0.125 MM | 0.125 MM |
| 100_DIFF_BGA | ISL9,ISL10 | Y | 0.075 MM | 0.075 MM | | 0.125 MM | 0.125 MM |

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

## PCB Rule Definitions

SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008


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APPLE INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7902 | D |

| SCALE | SHT | OF |
|---|---|---|
| NONE | 109 | 109 |

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